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1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.

2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.

3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHEM,EVT,MLB,K21

04/18/11

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REV

ECN

DESCRIPTION OF REVISION

CK APPD  
DATE

2011-04-18

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Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-8870	1	SCHEM,MLB,K21	SCH	CRITICAL	
#20-3023	1	PCBF,MLB,K21	PCB	CRITICAL	

DRAWING

TITLE-MLB

ABBREV-DRAWING

LAST MODIFIED: May 18 17:42:19 2011

PRODUCT SAFETY REQUIREMENTS:

PCB,UL RECOGNIZED, MIN. 130-C TEMP RATING AND V-O FLAME RATING PER UL 796 & UL 94  
PCB TO BE SILK-SCREENED WITH UL/CUL RECOGNITION MARK, MANUFACTURER'S UL FILE  
NUMBER, UL PCB MATERIAL DESIGNATION, 130-C TEMP RATING AND V-O FLAME RATING

DRAWING TITLE

SCHEM,MOCKUP,MLB,K21

Apple Inc.

051-8870

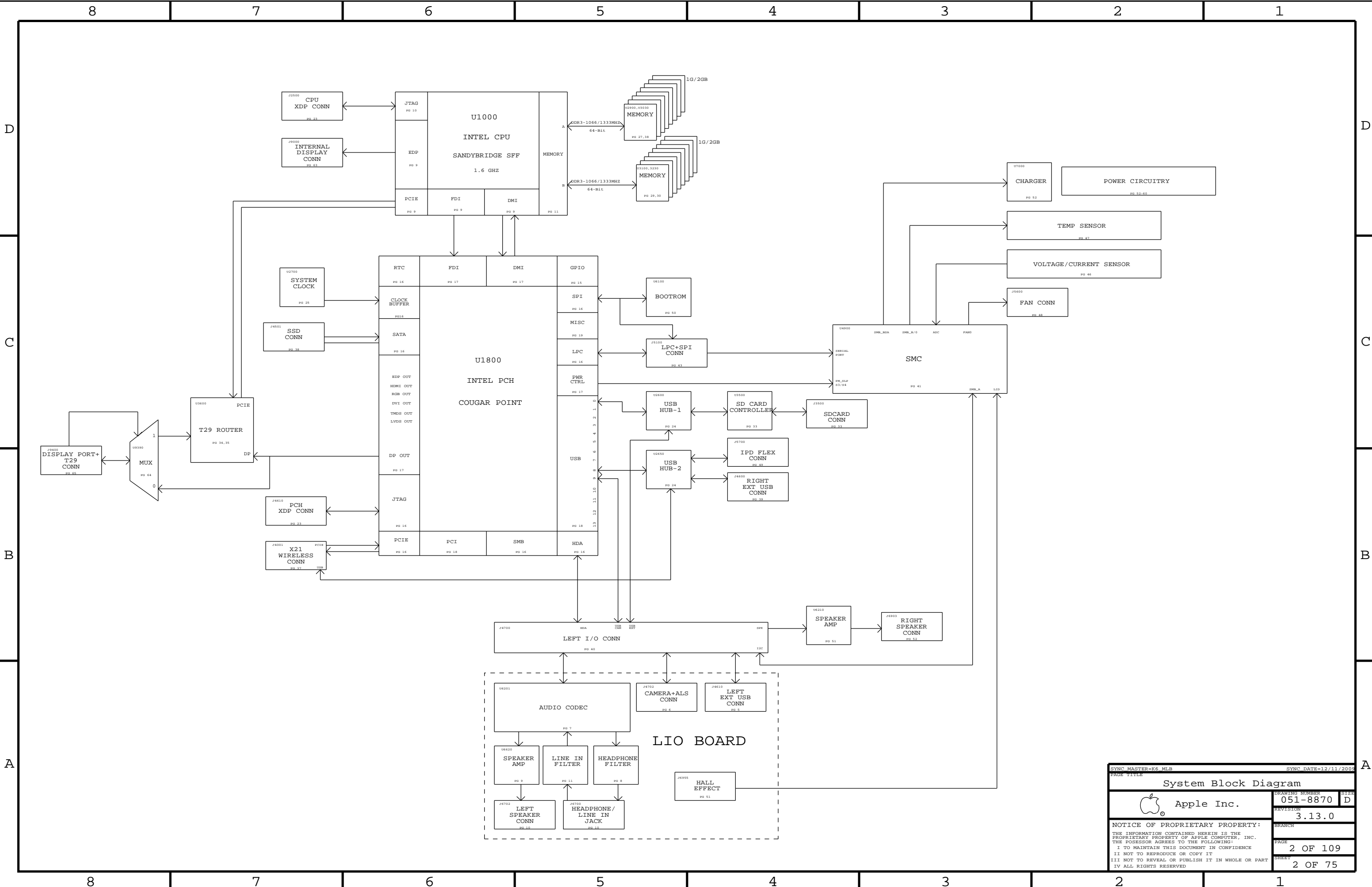
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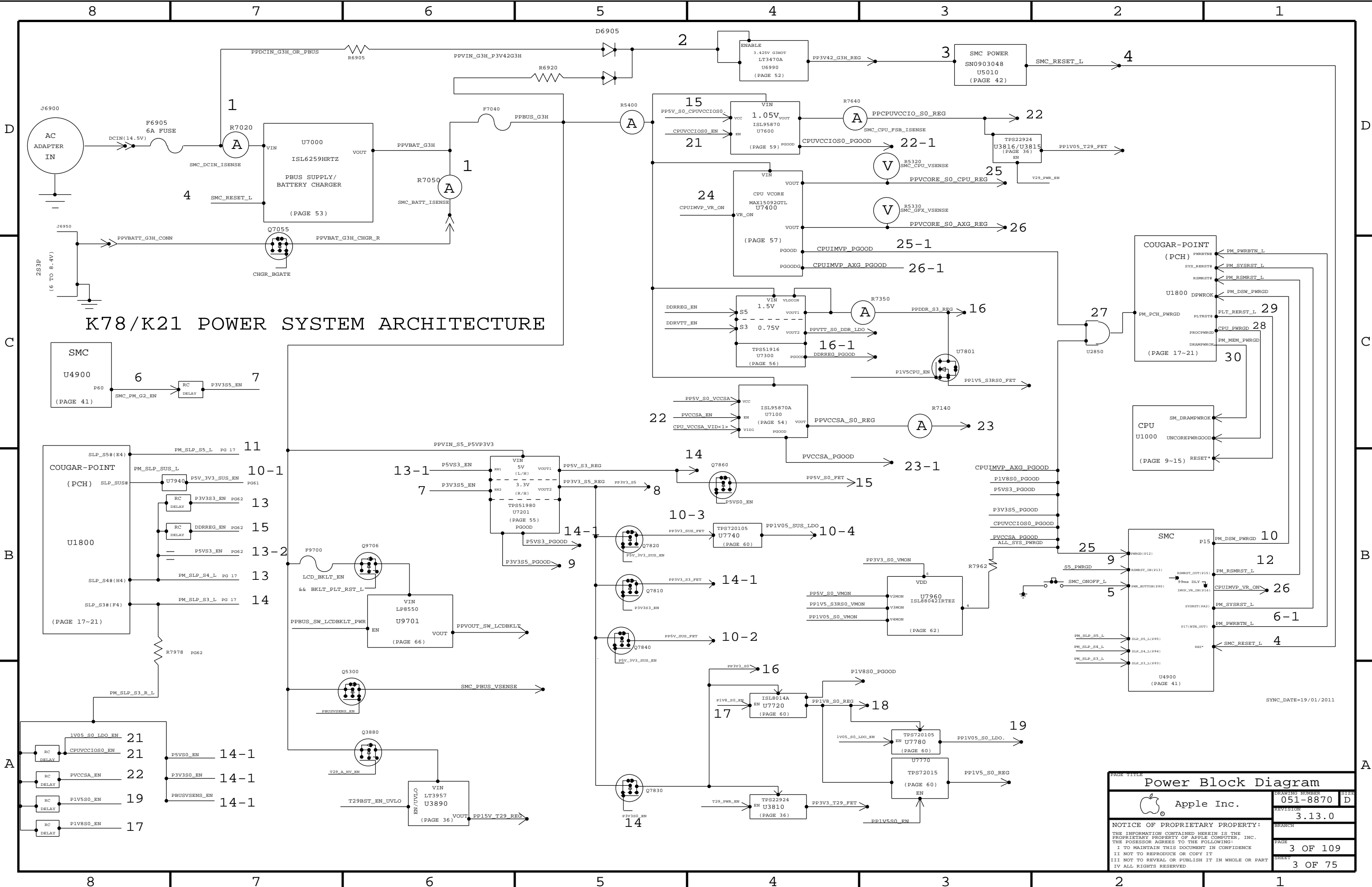
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K78/K21 POWER SYSTEM ARCHITECTURE

Power Block Diagram

Apple Inc.

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D	<div>BOM Variants</div> <table><tr><th>BOM NUMBER</th><th>BOM NAME</th><th>BOM OPTIONS</th></tr><tr><td>085-2684</td><td>K21i MLB DEVELOPMENT BOM</td><td>K21_DEVEL:ENG</td></tr><tr><td>607-8041</td><td>CMN PTS,PCBA,MLB,K21</td><td>K21_COMMON</td></tr><tr><td>639-2553</td><td>PCBA,MLB,1.8GHZ,NY 2GB,K21</td><td>K21_CMNPTS,EEEE:DP1P,CPU:1.8GHZ,DWR3:HYNIX_2GB</td></tr><tr><td>639-2554</td><td>PCBA,MLB,1.7GHZ,SA 4GB,K21</td><td>K21_CMNPTS,EEEE:DP1G,CPU:1.7GHZ,DWR3:SAMSUNG_4GB</td></tr><tr><td>639-2558</td><td>PCBA,MLB,1.8GHZ,EL 4GB,K21</td><td>K21_CMNPTS,EEEE:DP1H,CPU:1.8GHZ,DWR3:ELPIDA_4GB</td></tr><tr><td>639-2549</td><td>PCBA,MLB,1.7GHZ,EL 4GB,K21</td><td>K21_CMNPTS,EEEE:DP1J,CPU:1.7GHZ,DWR3:ELPIDA_4GB</td></tr><tr><td>639-2555</td><td>PCBA,MLB,1.8GHZ,NY 4GB,K21</td><td>K21_CMNPTS,EEEE:DP1K,CPU:1.8GHZ,DWR3:HYNIX_4GB</td></tr><tr><td>639-2557</td><td>PCBA,MLB,1.8GHZ,SA 4GB,K21</td><td>K21_CMNPTS,EEEE:DP1L,CPU:1.8GHZ,DWR3:SAMSUNG_4GB</td></tr><tr><td>639-2548</td><td>PCBA,MLB,1.7GHZ,NY 2GB,K21</td><td>K21_CMNPTS,EEEE:DP1M,CPU:1.7GHZ,DWR3:HYNIX_2GB</td></tr><tr><td>639-2550</td><td>PCBA,MLB,1.8GHZ,MI 2GB,K21</td><td>K21_CMNPTS,EEEE:DP1N,CPU:1.8GHZ,DWR3:MICRON_2GB</td></tr><tr><td>639-2551</td><td>PCBA,MLB,1.7GHZ,NY 4GB,K21</td><td>K21_CMNPTS,EEEE:DP1P,CPU:1.7GHZ,DWR3:HYNIX_4GB</td></tr><tr><td>639-2552</td><td>PCBA,MLB,1.7GHZ,SA 2GB,K21</td><td>K21_CMNPTS,EEEE:DP1Q,CPU:1.7GHZ,DWR3:SAMSUNG_2GB</td></tr><tr><td>639-2556</td><td>PCBA,MLB,1.8GHZ,SA 2GB,K21</td><td>K21_CMNPTS,EEEE:DP1R,CPU:1.8GHZ,DWR3:SAMSUNG_2GB</td></tr><tr><td>639-2559</td><td>PCBA,MLB,1.7GHZ,MI 2GB,K21</td><td>K21_CMNPTS,EEEE:DP1T,CPU:1.7GHZ,DWR3:MICRON_2GB</td></tr></table>								BOM NUMBER	BOM NAME	BOM OPTIONS	085-2684	K21i MLB DEVELOPMENT BOM	K21_DEVEL:ENG	607-8041	CMN PTS,PCBA,MLB,K21	K21_COMMON	639-2553	PCBA,MLB,1.8GHZ,NY 2GB,K21	K21_CMNPTS,EEEE:DP1P,CPU:1.8GHZ,DWR3:HYNIX_2GB	639-2554	PCBA,MLB,1.7GHZ,SA 4GB,K21	K21_CMNPTS,EEEE:DP1G,CPU:1.7GHZ,DWR3:SAMSUNG_4GB	639-2558	PCBA,MLB,1.8GHZ,EL 4GB,K21	K21_CMNPTS,EEEE:DP1H,CPU:1.8GHZ,DWR3:ELPIDA_4GB	639-2549	PCBA,MLB,1.7GHZ,EL 4GB,K21	K21_CMNPTS,EEEE:DP1J,CPU:1.7GHZ,DWR3:ELPIDA_4GB	639-2555	PCBA,MLB,1.8GHZ,NY 4GB,K21	K21_CMNPTS,EEEE:DP1K,CPU:1.8GHZ,DWR3:HYNIX_4GB	639-2557	PCBA,MLB,1.8GHZ,SA 4GB,K21	K21_CMNPTS,EEEE:DP1L,CPU:1.8GHZ,DWR3:SAMSUNG_4GB	639-2548	PCBA,MLB,1.7GHZ,NY 2GB,K21	K21_CMNPTS,EEEE:DP1M,CPU:1.7GHZ,DWR3:HYNIX_2GB	639-2550	PCBA,MLB,1.8GHZ,MI 2GB,K21	K21_CMNPTS,EEEE:DP1N,CPU:1.8GHZ,DWR3:MICRON_2GB	639-2551	PCBA,MLB,1.7GHZ,NY 4GB,K21	K21_CMNPTS,EEEE:DP1P,CPU:1.7GHZ,DWR3:HYNIX_4GB	639-2552	PCBA,MLB,1.7GHZ,SA 2GB,K21	K21_CMNPTS,EEEE:DP1Q,CPU:1.7GHZ,DWR3:SAMSUNG_2GB	639-2556	PCBA,MLB,1.8GHZ,SA 2GB,K21	K21_CMNPTS,EEEE:DP1R,CPU:1.8GHZ,DWR3:SAMSUNG_2GB	639-2559	PCBA,MLB,1.7GHZ,MI 2GB,K21	K21_CMNPTS,EEEE:DP1T,CPU:1.7GHZ,DWR3:MICRON_2GB	D
BOM NUMBER	BOM NAME	BOM OPTIONS																																																				
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639-2554	PCBA,MLB,1.7GHZ,SA 4GB,K21	K21_CMNPTS,EEEE:DP1G,CPU:1.7GHZ,DWR3:SAMSUNG_4GB																																																				
639-2558	PCBA,MLB,1.8GHZ,EL 4GB,K21	K21_CMNPTS,EEEE:DP1H,CPU:1.8GHZ,DWR3:ELPIDA_4GB																																																				
639-2549	PCBA,MLB,1.7GHZ,EL 4GB,K21	K21_CMNPTS,EEEE:DP1J,CPU:1.7GHZ,DWR3:ELPIDA_4GB																																																				
639-2555	PCBA,MLB,1.8GHZ,NY 4GB,K21	K21_CMNPTS,EEEE:DP1K,CPU:1.8GHZ,DWR3:HYNIX_4GB																																																				
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639-2556	PCBA,MLB,1.8GHZ,SA 2GB,K21	K21_CMNPTS,EEEE:DP1R,CPU:1.8GHZ,DWR3:SAMSUNG_2GB																																																				
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C									C																																													
B									B																																													
A	<div>Sub BOM</div> <table><tr><th>PART NUMBER</th><th>QTY</th><th>DESCRIPTION</th><th>REFERENCE DES</th><th>CRITICAL</th><th>BOM OPTION</th></tr><tr><td>085-2684</td><td>1</td><td>K21 MLB DEVELOPMENT</td><td>DEVEL</td><td>CRITICAL</td><td>DEVEL_BOM</td></tr><tr><td>607-8041</td><td>1</td><td>CMN PTS,PCBA,MLB,K21</td><td>CMNPTS</td><td>CRITICAL</td><td>K21_CMNPTS</td></tr></table>								PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	085-2684	1	K21 MLB DEVELOPMENT	DEVEL	CRITICAL	DEVEL_BOM	607-8041	1	CMN PTS,PCBA,MLB,K21	CMNPTS	CRITICAL	K21_CMNPTS	A																											
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607-8041	1	CMN PTS,PCBA,MLB,K21	CMNPTS	CRITICAL	K21_CMNPTS																																																	
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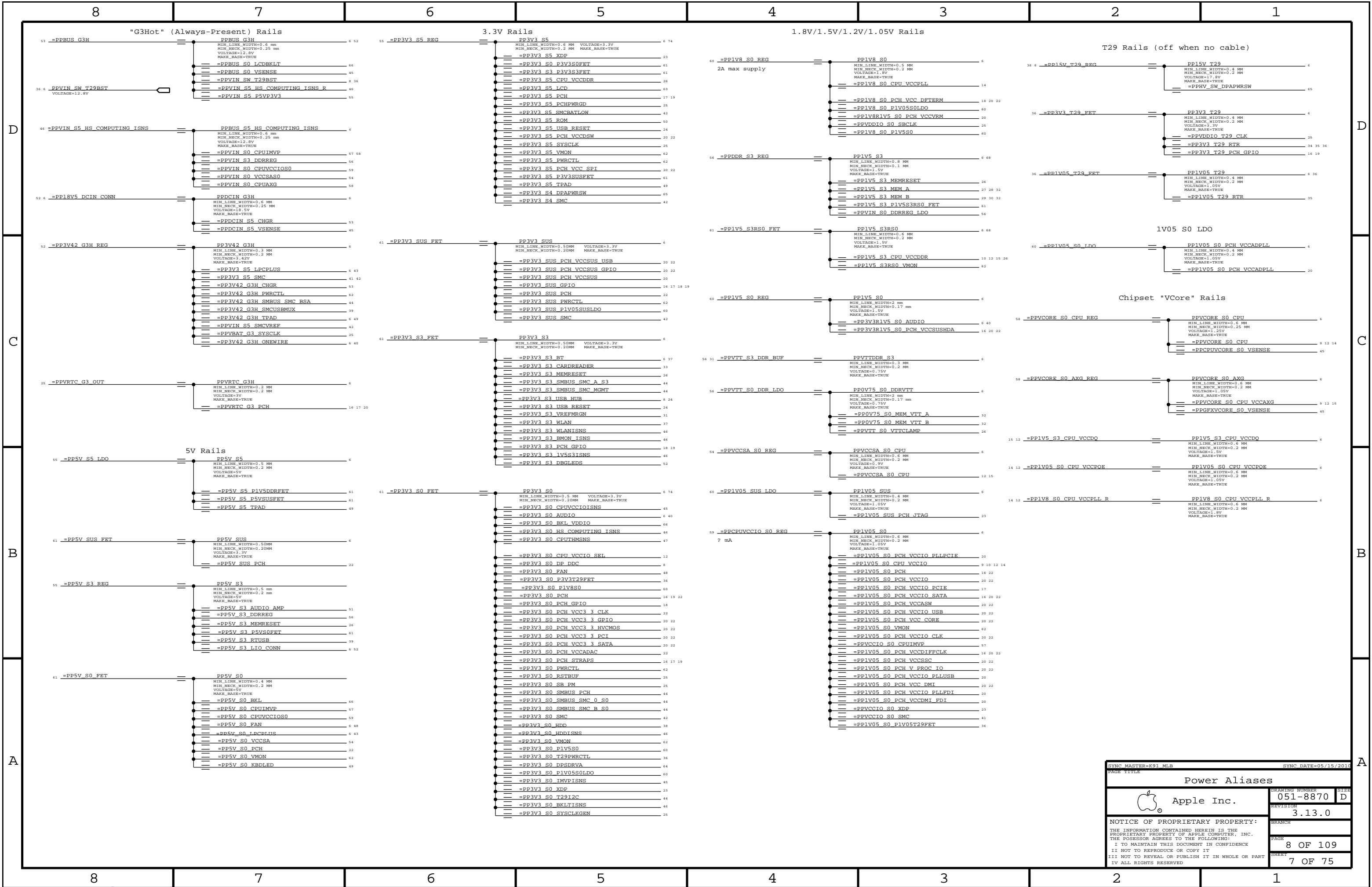
Bar Code Labels / EEEE #'s					
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
825-7563	1	LABEL,L10,K99	[EEEE:DP1P]	CRITICAL	EEEE:DP1P
825-7563	1	LABEL,L10,K99	[EEEE:DP1G]	CRITICAL	EEEE:DP1G
825-7563	1	LABEL,L10,K99	[EEEE:DP1H]	CRITICAL	EEEE:DP1H
825-7563	1	LABEL,L10,K99	[EEEE:DP1J]	CRITICAL	EEEE:DP1J
825-7563	1	LABEL,L10,K99	[EEEE:DP1K]	CRITICAL	EEEE:DP1K
825-7563	1	LABEL,L10,K99	[EEEE:DP1L]	CRITICAL	EEEE:DP1L
825-7563	1	LABEL,L10,K99	[EEEE:DP1M]	CRITICAL	EEEE:DP1M
825-7563	1	LABEL,L10,K99	[EEEE:DP1N]	CRITICAL	EEEE:DP1N
825-7563	1	LABEL,L10,K99	[EEEE:DP1P]	CRITICAL	EEEE:DP1P
825-7563	1	LABEL,L10,K99	[EEEE:DP1Q]	CRITICAL	EEEE:DP1Q
825-7563	1	LABEL,L10,K99	[EEEE:DP1R]	CRITICAL	EEEE:DP1R
825-7563	1	LABEL,L10,K99	[EEEE:DP1T]	CRITICAL	EEEE:DP1T

SYNC MASTER=MASTER		SYNC DATE=MASTER	
PAGE TITLE			
Revision History			
 Apple Inc.		DRAWING NUMBER	051-8870
		REVISION	3.13.0
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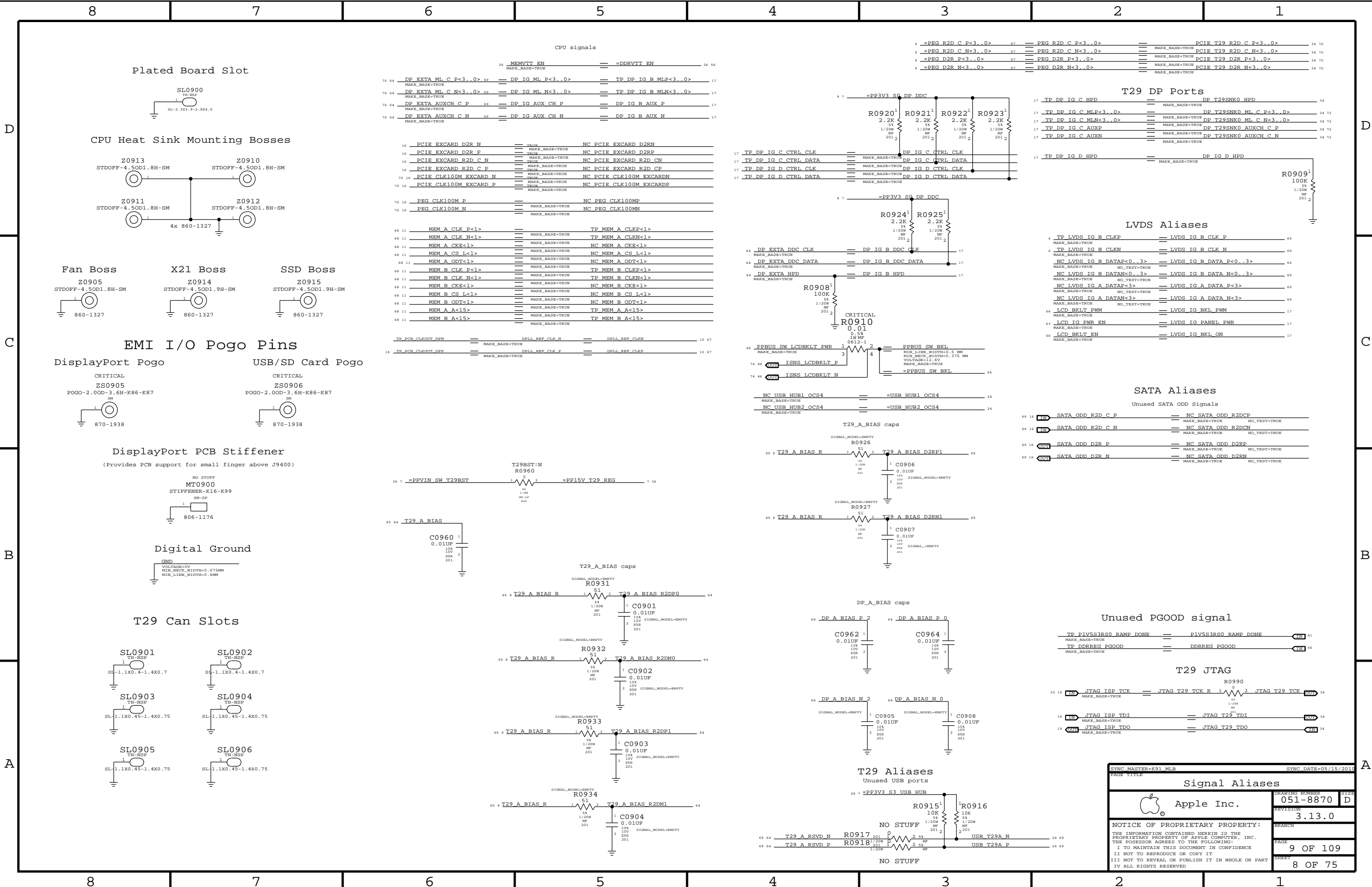
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K21 BOM GROUPS																																																																																																																																																													
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K21_COMMON	ALTERNATE,COMMON,K21_MISC,K21_DEBUG:ENG,K21_PROGPARTS,USBHUB_2513B,T29BST:Y,EDP,PCB:B3																																																																																																																																																												
K21_MISC	CPUMEM_80,MB1_2NONRES,MB2_2NONRES,T29:YES,SDRV12C:MCU,SDRV_PD,K8_BL																																																																																																																																																												
K21_PROGPARTS	BOOTROM_PROD,SMC_PROD,T29ROM:PROD,T29MCU:PROD																																																																																																																																																												
K21_DEVEL:ENG	BELT:ENG,BMON:ENG,XDP_CONN,XDP_CPU:BPW,XDP_PCH,LPCPLUS,VREFPMON,SOPGOOD_1SL,S3_S0_LSD,VOCIOISNS_ENG,AIRPORTISNS_ENG,SDIOISNS_ENG,LCDBELTISNS_ENG																																																																																																																																																												
K21_DEVEL:PVT	LCPPLUS_XDP_CONN,XDP_PCH																																																																																																																																																												
K21_DEBUG:ENG	DEVEL_BOM,SMC_DEBUG_YES,XDP																																																																																																																																																												
K21_DEBUG:PVT	DEVEL_BOM,BELT:PROD,BMON:PROD,SMC_DEBUG_YES,XDP,VREFPMON_NOT																																																																																																																																																												
K21_DEBUG:PROD	BELT:PROD,BMON:PROD,SMC_DEBUG_YES,XDP,VREFPMON_NOT,LCPPLUS,VOCIOISNS_PROD,AIRPORTISNS_PROD,SDIOISNS_PROD,LCDBELTISNS_PROD																																																																																																																																																												
DDR3:HYNIX_2GB	DRAM_CFG0:L,DRAM_CFG1:L,DRAM_CFG2:L,DRAM_CFG3:L,DRAM_TYPE:HYNIX_2GB																																																																																																																																																												
DDR3:HYNIX_4GB	DRAM_CFG0:L,DRAM_CFG1:L,DRAM_CFG2:H,DRAM_CFG3:L,DRAM_TYPE:HYNIX_4GB																																																																																																																																																												
DDR3:SAMSUNG_2GB	DRAM_CFG0:L,DRAM_CFG1:H,DRAM_CFG2:L,DRAM_CFG3:L,DRAM_TYPE:SAMSUNG_2GB																																																																																																																																																												
DDR3:SAMSUNG_4GB	DRAM_CFG0:L,DRAM_CFG1:H,DRAM_CFG2:H,DRAM_CFG3:L,DRAM_TYPE:SAMSUNG_4GB																																																																																																																																																												
DDR3:MICRON_2GB	DRAM_CFG0:H,DRAM_CFG1:L,DRAM_CFG2:L,DRAM_CFG3:L,DRAM_TYPE:MICRON_2GB																																																																																																																																																												
DDR3:ELPIDA_4GB	DRAM_CFG0:H,DRAM_CFG1:H,DRAM_CFG2:H,DRAM_CFG3:L,DRAM_TYPE:ELPIDA_4GB																																																																																																																																																												
Module Parts																																																																																																																																																													
<table><tr><th>PART NUMBER</th><th>QTY</th><th>DESCRIPTION</th><th>REFERENCE DES</th><th>CRITICAL</th><th>BOM OPTION</th></tr><tr><td>337S4121</td><td>1</td><td>SNB,QAYS,QS,J1.1.8,17W,2+2,1.20,4M,BGA</td><td>U1000</td><td>CRITICAL</td><td>CPU:1.8GHZ</td></tr><tr><td>337S4119</td><td>1</td><td>SNB,QAYH,QS,J1.1.7,17W,2+2,1.20,3M,BGA</td><td>U1000</td><td>CRITICAL</td><td>CPU:1.7GHZ</td></tr><tr><td>337S4101</td><td>1</td><td>SNB,QAM1,QS,J1.1.6,17W,2+2,1.1,4M,BGA</td><td>U1000</td><td>CRITICAL</td><td>CPU:1.6GHZ</td></tr><tr><td>337S4100</td><td>1</td><td>SNB,QAM2,QS,J1.1.5,17W,2+2,1.1,4M,BGA</td><td>U1000</td><td>CRITICAL</td><td>CPU:1.5GHZ</td></tr><tr><td>337S4099</td><td>1</td><td>SNB,QAM3,QS,J1.1.4,17W,2+2,1.05,3M,BGA</td><td>U1000</td><td>CRITICAL</td><td>CPU:1.4GHZ</td></tr><tr><td>337S4098</td><td>1</td><td>SNB,QAYV,QS,J1.1.3,17W,2+2,1.05,3M,BGA</td><td>U1000</td><td>CRITICAL</td><td>CPU:1.3GHZ</td></tr><tr><td>337S4080</td><td>1</td><td>COUGAR POINT,SLHAG,FRQ,8082Q567</td><td>U1800</td><td>CRITICAL</td><td>PCB:B2</td></tr><tr><td>337S4091</td><td>1</td><td>COUGAR POINT,B3,SL74K,FRQ,8082Q567</td><td>U1800</td><td>CRITICAL</td><td>PCB:B3</td></tr></table>								PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	337S4121	1	SNB,QAYS,QS,J1.1.8,17W,2+2,1.20,4M,BGA	U1000	CRITICAL	CPU:1.8GHZ	337S4119	1	SNB,QAYH,QS,J1.1.7,17W,2+2,1.20,3M,BGA	U1000	CRITICAL	CPU:1.7GHZ	337S4101	1	SNB,QAM1,QS,J1.1.6,17W,2+2,1.1,4M,BGA	U1000	CRITICAL	CPU:1.6GHZ	337S4100	1	SNB,QAM2,QS,J1.1.5,17W,2+2,1.1,4M,BGA	U1000	CRITICAL	CPU:1.5GHZ	337S4099	1	SNB,QAM3,QS,J1.1.4,17W,2+2,1.05,3M,BGA	U1000	CRITICAL	CPU:1.4GHZ	337S4098	1	SNB,QAYV,QS,J1.1.3,17W,2+2,1.05,3M,BGA	U1000	CRITICAL	CPU:1.3GHZ	337S4080	1	COUGAR POINT,SLHAG,FRQ,8082Q567	U1800	CRITICAL	PCB:B2	337S4091	1	COUGAR POINT,B3,SL74K,FRQ,8082Q567	U1800	CRITICAL	PCB:B3																																																																																																
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<table><tr><td>338S0976</td><td>1</td><td>IC,T29 Eagle Ridge,192 PCBGA,8x9MM</td><td>U3600</td><td>CRITICAL</td><td>T29:YES</td></tr><tr><td>333S0585</td><td>4</td><td>IC,SDRAM,1GBIT,DDR3-1333,76P FBGA,T-DIE,HYNIX</td><td>U2900,U2910,U2920,U2930</td><td>CRITICAL</td><td>DRAM_TYPE:HYNIX_2GB</td></tr><tr><td>333S0585</td><td>4</td><td>IC,SDRAM,1GBIT,DDR3-1333,76P FBGA,T-DIE,HYNIX</td><td>U3000,U3010,U3020,U3030</td><td>CRITICAL</td><td>DRAM_TYPE:HYNIX_2GB</td></tr><tr><td>333S0585</td><td>4</td><td>IC,SDRAM,1GBIT,DDR3-1333,76P FBGA,T-DIE,HYNIX</td><td>U3100,U3110,U3120,U3130</td><td>CRITICAL</td><td>DRAM_TYPE:HYNIX_2GB</td></tr><tr><td>333S0585</td><td>4</td><td>IC,SDRAM,1GBIT,DDR3-1333,76P FBGA,T-DIE,HYNIX</td><td>U3200,U3210,U3220,U3230</td><td>CRITICAL</td><td>DRAM_TYPE:HYNIX_2GB</td></tr><tr><td>333S0586</td><td>4</td><td>IC,SDRAM,2GBIT,DDR3-1333,76P FBGA,B-DIE,HYNIX</td><td>U2900,U2910,U2920,U2930</td><td>CRITICAL</td><td>DRAM_TYPE:HYNIX_4GB</td></tr><tr><td>333S0586</td><td>4</td><td>IC,SDRAM,2GBIT,DDR3-1333,76P FBGA,B-DIE,HYNIX</td><td>U3000,U3010,U3020,U3030</td><td>CRITICAL</td><td>DRAM_TYPE:HYNIX_4GB</td></tr><tr><td>333S0586</td><td>4</td><td>IC,SDRAM,2GBIT,DDR3-1333,76P FBGA,B-DIE,HYNIX</td><td>U3100,U3110,U3120,U3130</td><td>CRITICAL</td><td>DRAM_TYPE:HYNIX_4GB</td></tr><tr><td>333S0586</td><td>4</td><td>IC,SDRAM,2GBIT,DDR3-1333,76P FBGA,B-DIE,HYNIX</td><td>U3200,U3210,U3220,U3230</td><td>CRITICAL</td><td>DRAM_TYPE:HYNIX_4GB</td></tr><tr><td>333S0587</td><td>4</td><td>IC,SDRAM,1GBIT,DDR3-1333,76P FBGA,Q-DIE,SAMSUNG</td><td>U2900,U2910,U2920,U2930</td><td>CRITICAL</td><td>DRAM_TYPE:SAMSUNG_2GB</td></tr><tr><td>333S0587</td><td>4</td><td>IC,SDRAM,1GBIT,DDR3-1333,76P FBGA,Q-DIE,SAMSUNG</td><td>U3000,U3010,U3020,U3030</td><td>CRITICAL</td><td>DRAM_TYPE:SAMSUNG_2GB</td></tr><tr><td>333S0587</td><td>4</td><td>IC,SDRAM,1GBIT,DDR3-1333,76P FBGA,Q-DIE,SAMSUNG</td><td>U3100,U3110,U3120,U3130</td><td>CRITICAL</td><td>DRAM_TYPE:SAMSUNG_2GB</td></tr><tr><td>333S0587</td><td>4</td><td>IC,SDRAM,1GBIT,DDR3-1333,76P FBGA,Q-DIE,SAMSUNG</td><td>U3200,U3210,U3220,U3230</td><td>CRITICAL</td><td>DRAM_TYPE:SAMSUNG_2GB</td></tr><tr><td>333S0588</td><td>4</td><td>IC,SDRAM,2GBIT,DDR3-1333,76P FBGA,D-DIE,SAMSUNG</td><td>U3000,U3010,U3020,U3030</td><td>CRITICAL</td><td>DRAM_TYPE:SAMSUNG_4GB</td></tr><tr><td>333S0588</td><td>4</td><td>IC,SDRAM,2GBIT,DDR3-1333,76P FBGA,D-DIE,SAMSUNG</td><td>U3100,U3110,U3120,U3130</td><td>CRITICAL</td><td>DRAM_TYPE:SAMSUNG_4GB</td></tr><tr><td>333S0588</td><td>4</td><td>IC,SDRAM,2GBIT,DDR3-1333,76P FBGA,D-DIE,SAMSUNG</td><td>U3200,U3210,U3220,U3230</td><td>CRITICAL</td><td>DRAM_TYPE:SAMSUNG_4GB</td></tr><tr><td>333S0590</td><td>4</td><td>IC,SDRAM,1GBIT,DDR3-1333,76P FBGA,V68A-D,MICRON</td><td>U2900,U2910,U2920,U2930</td><td>CRITICAL</td><td>DRAM_TYPE:MICRON_2GB</td></tr><tr><td>333S0590</td><td>4</td><td>IC,SDRAM,1GBIT,DDR3-1333,76P FBGA,V68A-D,MICRON</td><td>U3000,U3010,U3020,U3030</td><td>CRITICAL</td><td>DRAM_TYPE:MICRON_2GB</td></tr><tr><td>333S0590</td><td>4</td><td>IC,SDRAM,1GBIT,DDR3-1333,76P FBGA,V68A-D,MICRON</td><td>U3100,U3110,U3120,U3130</td><td>CRITICAL</td><td>DRAM_TYPE:MICRON_2GB</td></tr><tr><td>333S0590</td><td>4</td><td>IC,SDRAM,1GBIT,DDR3-1333,76P FBGA,V68A-D,MICRON</td><td>U3200,U3210,U3220,U3230</td><td>CRITICAL</td><td>DRAM_TYPE:MICRON_2GB</td></tr><tr><td>333S0589</td><td>4</td><td>IC,SDRAM,2GBIT,DDR3-1333,76P FBGA,C-DIE,ELPIDA</td><td>U2900,U2910,U2920,U2930</td><td>CRITICAL</td><td>DRAM_TYPE:ELPIDA_4GB</td></tr><tr><td>333S0589</td><td>4</td><td>IC,SDRAM,2GBIT,DDR3-1333,76P FBGA,C-DIE,ELPIDA</td><td>U3000,U3010,U3020,U3030</td><td>CRITICAL</td><td>DRAM_TYPE:ELPIDA_4GB</td></tr><tr><td>333S0589</td><td>4</td><td>IC,SDRAM,2GBIT,DDR3-1333,76P FBGA,C-DIE,ELPIDA</td><td>U3100,U3110,U3120,U3130</td><td>CRITICAL</td><td>DRAM_TYPE:ELPIDA_4GB</td></tr><tr><td>333S0589</td><td>4</td><td>IC,SDRAM,2GBIT,DDR3-1333,76P FBGA,C-DIE,ELPIDA</td><td>U3200,U3210,U3220,U3230</td><td>CRITICAL</td><td>DRAM_TYPE:ELPIDA_4GB</td></tr><tr><td>353s2929</td><td>1</td><td>IC,1SL6259,BATCHARGER,3%,4X4MM,QFN28</td><td>U7000</td><td>CRITICAL</td><td></td></tr></table>								338S0976	1	IC,T29 Eagle Ridge,192 PCBGA,8x9MM	U3600	CRITICAL	T29:YES	333S0585	4	IC,SDRAM,1GBIT,DDR3-1333,76P FBGA,T-DIE,HYNIX	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:HYNIX_2GB	333S0585	4	IC,SDRAM,1GBIT,DDR3-1333,76P FBGA,T-DIE,HYNIX	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:HYNIX_2GB	333S0585	4	IC,SDRAM,1GBIT,DDR3-1333,76P FBGA,T-DIE,HYNIX	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:HYNIX_2GB	333S0585	4	IC,SDRAM,1GBIT,DDR3-1333,76P FBGA,T-DIE,HYNIX	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:HYNIX_2GB	333S0586	4	IC,SDRAM,2GBIT,DDR3-1333,76P FBGA,B-DIE,HYNIX	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:HYNIX_4GB	333S0586	4	IC,SDRAM,2GBIT,DDR3-1333,76P FBGA,B-DIE,HYNIX	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:HYNIX_4GB	333S0586	4	IC,SDRAM,2GBIT,DDR3-1333,76P FBGA,B-DIE,HYNIX	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:HYNIX_4GB	333S0586	4	IC,SDRAM,2GBIT,DDR3-1333,76P FBGA,B-DIE,HYNIX	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:HYNIX_4GB	333S0587	4	IC,SDRAM,1GBIT,DDR3-1333,76P FBGA,Q-DIE,SAMSUNG	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:SAMSUNG_2GB	333S0587	4	IC,SDRAM,1GBIT,DDR3-1333,76P FBGA,Q-DIE,SAMSUNG	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:SAMSUNG_2GB	333S0587	4	IC,SDRAM,1GBIT,DDR3-1333,76P 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FBGA,V68A-D,MICRON	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:MICRON_2GB	333S0589	4	IC,SDRAM,2GBIT,DDR3-1333,76P FBGA,C-DIE,ELPIDA	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:ELPIDA_4GB	333S0589	4	IC,SDRAM,2GBIT,DDR3-1333,76P FBGA,C-DIE,ELPIDA	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:ELPIDA_4GB	333S0589	4	IC,SDRAM,2GBIT,DDR3-1333,76P FBGA,C-DIE,ELPIDA	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:ELPIDA_4GB	333S0589	4	IC,SDRAM,2GBIT,DDR3-1333,76P FBGA,C-DIE,ELPIDA	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:ELPIDA_4GB	353s2929	1	IC,1SL6259,BATCHARGER,3%,4X4MM,QFN28	U7000	CRITICAL	
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333S0587	4	IC,SDRAM,1GBIT,DDR3-1333,76P FBGA,Q-DIE,SAMSUNG	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:SAMSUNG_2GB																																																																																																																																																								
333S0588	4	IC,SDRAM,2GBIT,DDR3-1333,76P FBGA,D-DIE,SAMSUNG	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:SAMSUNG_4GB																																																																																																																																																								
333S0588	4	IC,SDRAM,2GBIT,DDR3-1333,76P FBGA,D-DIE,SAMSUNG	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:SAMSUNG_4GB																																																																																																																																																								
333S0588	4	IC,SDRAM,2GBIT,DDR3-1333,76P FBGA,D-DIE,SAMSUNG	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:SAMSUNG_4GB																																																																																																																																																								
333S0590	4	IC,SDRAM,1GBIT,DDR3-1333,76P FBGA,V68A-D,MICRON	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:MICRON_2GB																																																																																																																																																								
333S0590	4	IC,SDRAM,1GBIT,DDR3-1333,76P FBGA,V68A-D,MICRON	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:MICRON_2GB																																																																																																																																																								
333S0590	4	IC,SDRAM,1GBIT,DDR3-1333,76P FBGA,V68A-D,MICRON	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:MICRON_2GB																																																																																																																																																								
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333S0589	4	IC,SDRAM,2GBIT,DDR3-1333,76P FBGA,C-DIE,ELPIDA	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:ELPIDA_4GB																																																																																																																																																								
333S0589	4	IC,SDRAM,2GBIT,DDR3-1333,76P FBGA,C-DIE,ELPIDA	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:ELPIDA_4GB																																																																																																																																																								
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353s2929	1	IC,1SL6259,BATCHARGER,3%,4X4MM,QFN28	U7000	CRITICAL																																																																																																																																																									
PD Module Parts																																																																																																																																																													
<table><tr><td>806-2333</td><td>1</td><td>K21, T29 Fence</td><td>T29FENCE</td><td>CRITICAL</td><td></td></tr><tr><td>806-2356</td><td>1</td><td>K21, T29 Can</td><td>T29CAN</td><td>CRITICAL</td><td>NOSTUFF</td></tr><tr><td>806-2347</td><td>1</td><td>K21, T29 Filter Can</td><td>T29FILTERCAN</td><td>CRITICAL</td><td></td></tr><tr><td>806-2376</td><td>1</td><td>K78, mDP Can</td><td>MDPCAN</td><td>CRITICAL</td><td></td></tr><tr><td>806-2377</td><td>1</td><td>K78, mDP Spring</td><td>MDPSPRING</td><td>CRITICAL</td><td>NOSTUFF</td></tr></table>								806-2333	1	K21, T29 Fence	T29FENCE	CRITICAL		806-2356	1	K21, T29 Can	T29CAN	CRITICAL	NOSTUFF	806-2347	1	K21, T29 Filter Can	T29FILTERCAN	CRITICAL		806-2376	1	K78, mDP Can	MDPCAN	CRITICAL		806-2377	1	K78, mDP Spring	MDPSPRING	CRITICAL	NOSTUFF																																																																																																																								
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<table><tr><th>VENDOR</th><th>CFG 1</th><th>CFG 0</th></tr><tr><td>HYNIX</td><td>0</td><td>0</td></tr><tr><td>SAMSUNG</td><td>1</td><td>0</td></tr><tr><td>MICRON</td><td>0</td><td>1</td></tr><tr><td>ELPIDA</td><td>1</td><td>1</td></tr></table>								VENDOR	CFG 1	CFG 0	HYNIX	0	0	SAMSUNG	1	0	MICRON	0	1	ELPIDA	1	1																																																																																																																																							
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<table><tr><th>SIZE</th><th>CFG 2</th><th>DIE REV</th><th>CFG 3</th></tr><tr><td>2GB</td><td>0</td><td>A</td><td>0</td></tr><tr><td>4GB</td><td>1</td><td>B</td><td>1</td></tr></table>								SIZE	CFG 2	DIE REV	CFG 3	2GB	0	A	0	4GB	1	B	1																																																																																																																																										
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8	7	6	5	4	3	2	1
Functional Test Points							
J4001: AirPort / BT Connector		J5600: Fan Connector		J5715: KB BKLT CONNECTOR			
FUNC_TEST		FUNC_TEST		FUNC_TEST			
TRUE PP3V3 WLAN F 37 (Need 5 TPs)		TRUE =PP5V_S0_FAN 7 48		TRUE KBDLED_FB 49		NC EDP TXP<0..3> TRUE == TP EDP TX P<0..3> 9	
TRUE WIFI_EVENT_L 37 41		TRUE FAN_RT_TACH 48		TRUE KBDLED_ANODE 49		MAKE_BASE=TRUE TP EDP TX N<0..3> 9	
TRUE PCIE AP_R2D_N 37 70		TRUE FAN_RT_PWM 48		(Need to add 2 GND TP)		NC EDP_AUXN MAKE_BASE=TRUE TP EDP AUX P	
TRUE PCIE AP_R2D_P 37 70		(Need to add 1 GND TP)				MAKE_BASE=TRUE TP CPU THERMDA	
TRUE PCIE CLK100M_AP_N 16 37 70		J5700: IPD Flex Connector				NC CPU THERMDC TRUE TP CPU THERMDC	
TRUE PCIE CLK100M_AP_P 16 37 70		FUNC_TEST				NC CPU RSVD<30..45> TRUE TP CPU RSVD<30..45>	
TRUE USB_BT_P 24 37 69		B999 TRUE PP3V3_TPAD_CONN 49				MAKE_BASE=TRUE TP CPU RSVD<8..27> 9	
TRUE USB_BT_N 24 37 69		TRUE PP5V_TPAD_FILT 49					
TRUE PCIE AP_D2R_P 16 37 70		TRUE =PP3V42_G3H_TPAD 7 49					
TRUE PCIE AP_D2R_N 16 37 70		TRUE USB_TPAD_CONN_P 49 74					
TRUE PCIE_WAKE_L 17 37		TRUE USB_TPAD_CONN_N 49 74					
TRUE AP_RESET_CONN_L 37		TRUE =I2C_TPAD_SDA 44 49					
TRUE AP_CLKREQ_O_L 37		TRUE =I2C_TPAD_SCL 44 49					
TRUE =PP3V3_S3_BT 7 37		TRUE SMC_ONOFF_L 41 42 49					
(Need to add 8 GND TPs)		TRUE SMC_LID 6 40 41 42 49					
		TRUE SMC_TPAD_RST_L 42 49					
		B999 TRUE SMC_PME_S4_WAKE_L 41 42 49					
		(Need to add 5 GND TPs)					
		J6900: DC-In Connector					
		FUNC_TEST					
		TRUE =PP18V5_DCIN_CONN 7 52 (Need 6 TPs)					
		TRUE =PP5V_S3_LIO_CONN 7 52					
		(Need to add 5 GND TPs)					
		J6903: Speaker Connector					
		FUNC_TEST					
		TRUE SPKRAMP_R_P_OUT 51 52 74					
		TRUE SPKRAMP_R_N_OUT 51 52 74					
		(Need to add 3 GND TPs)					
		J6950: Battery Connector					
		FUNC_TEST					
		TRUE PPVBAT_G3H_CONN 52 53 (Need 4 TPs)					
		TRUE =SMBUS_BATT_SCL 44 52					
		TRUE =SMBUS_BATT_SDA 44 52					
		TRUE SYS_DETECT_L 52					
		(Need to add 4 GND TPs near J6950 and 1 for shield)					
		J9000: Internal DP Connector					
		FUNC_TEST					
		TRUE PPVOUT_SW_LCDBKLT 63 66 (Need 2 TPs)					
		TRUE PP3V3_SW_LCD 63					
		TRUE I2C_TCON_SDA_R 63					
		TRUE I2C_TCON_SCL_R 63					
		(Need 2 TPs)					





SYNC MASTER=K91 MLB		SYNC DATE=05/15/2010	
PAGE TITLE		PAGE	
Power Aliases		DRAWING NUMBER	SIZE
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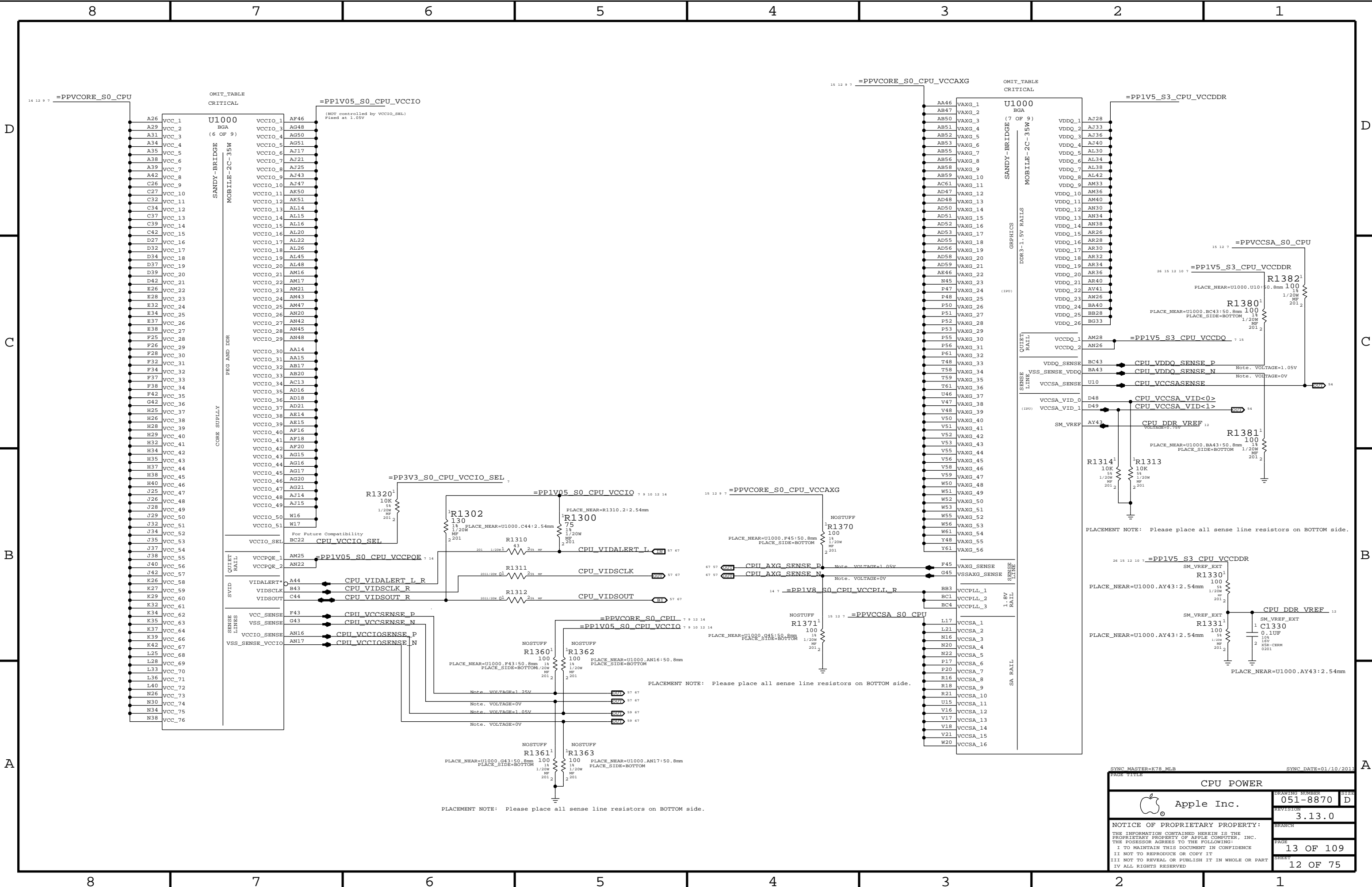







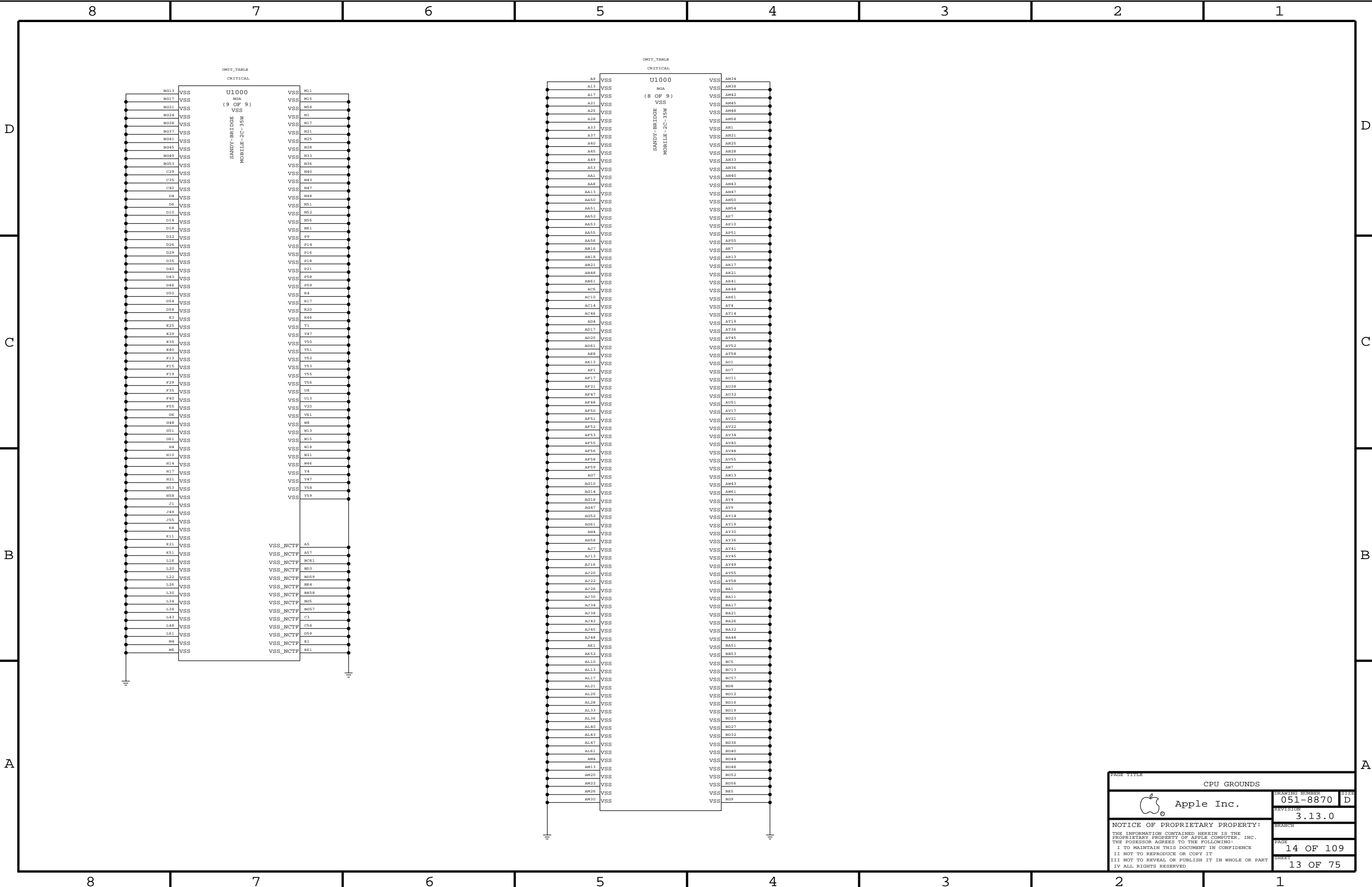




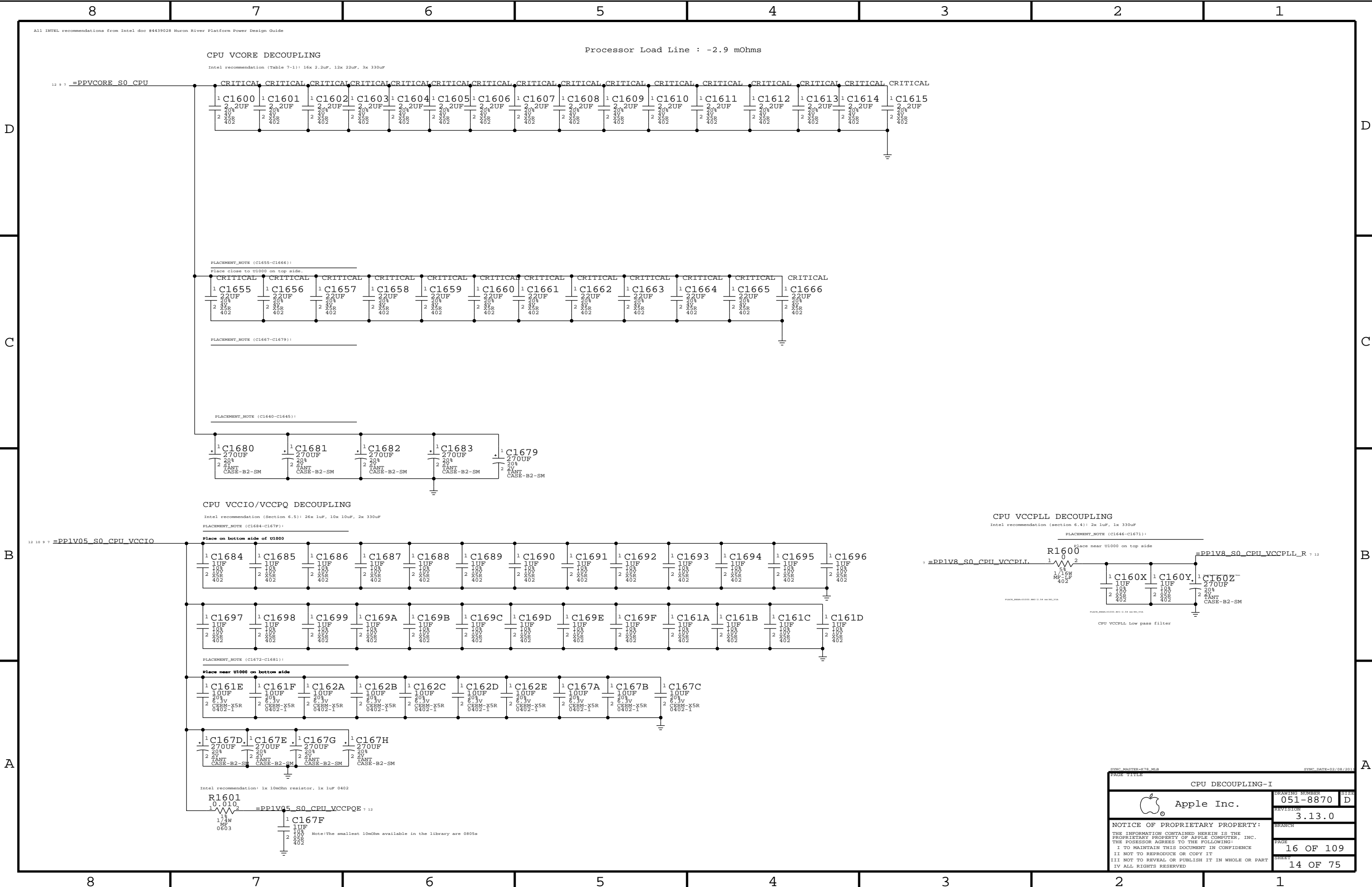


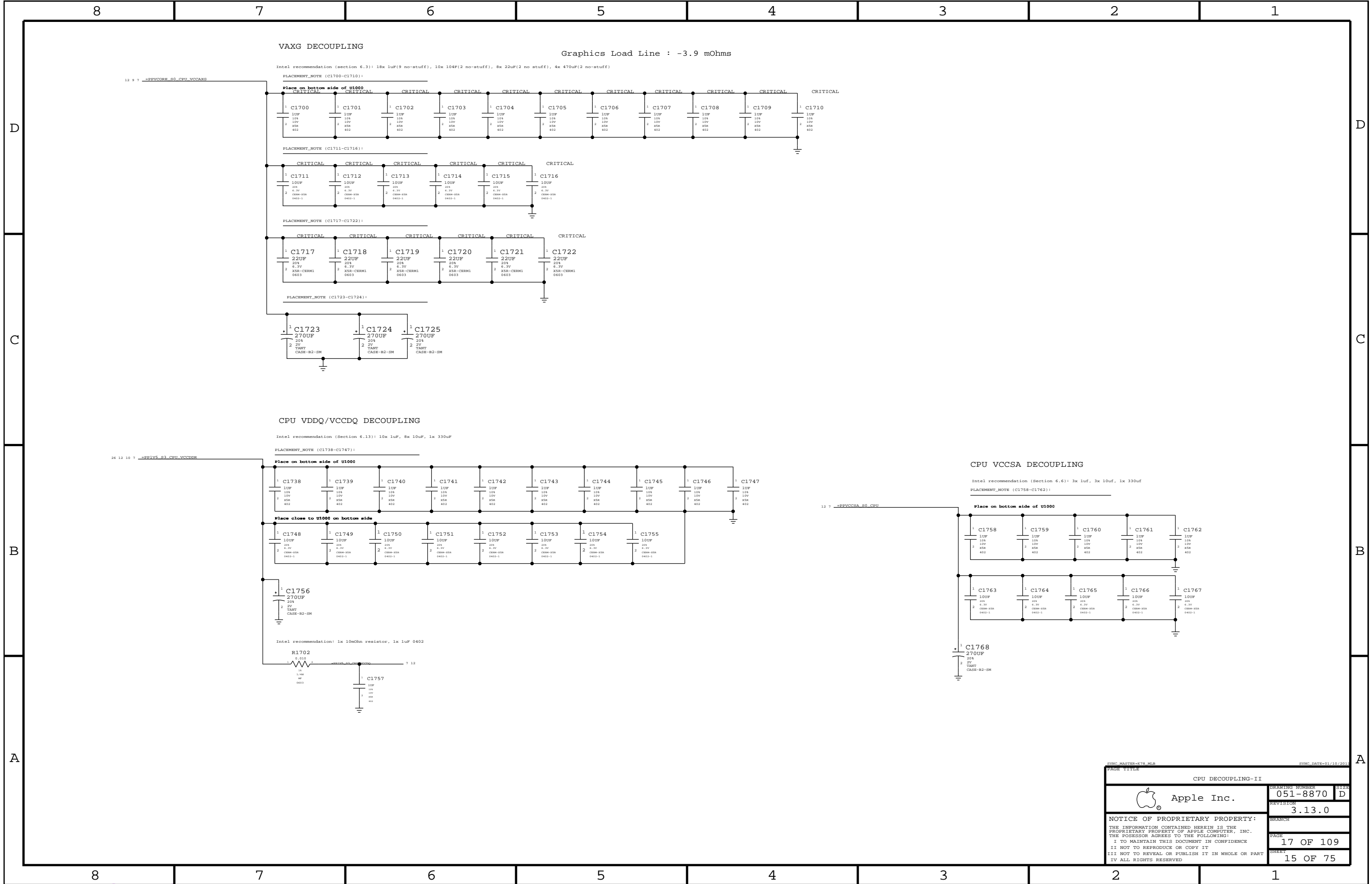
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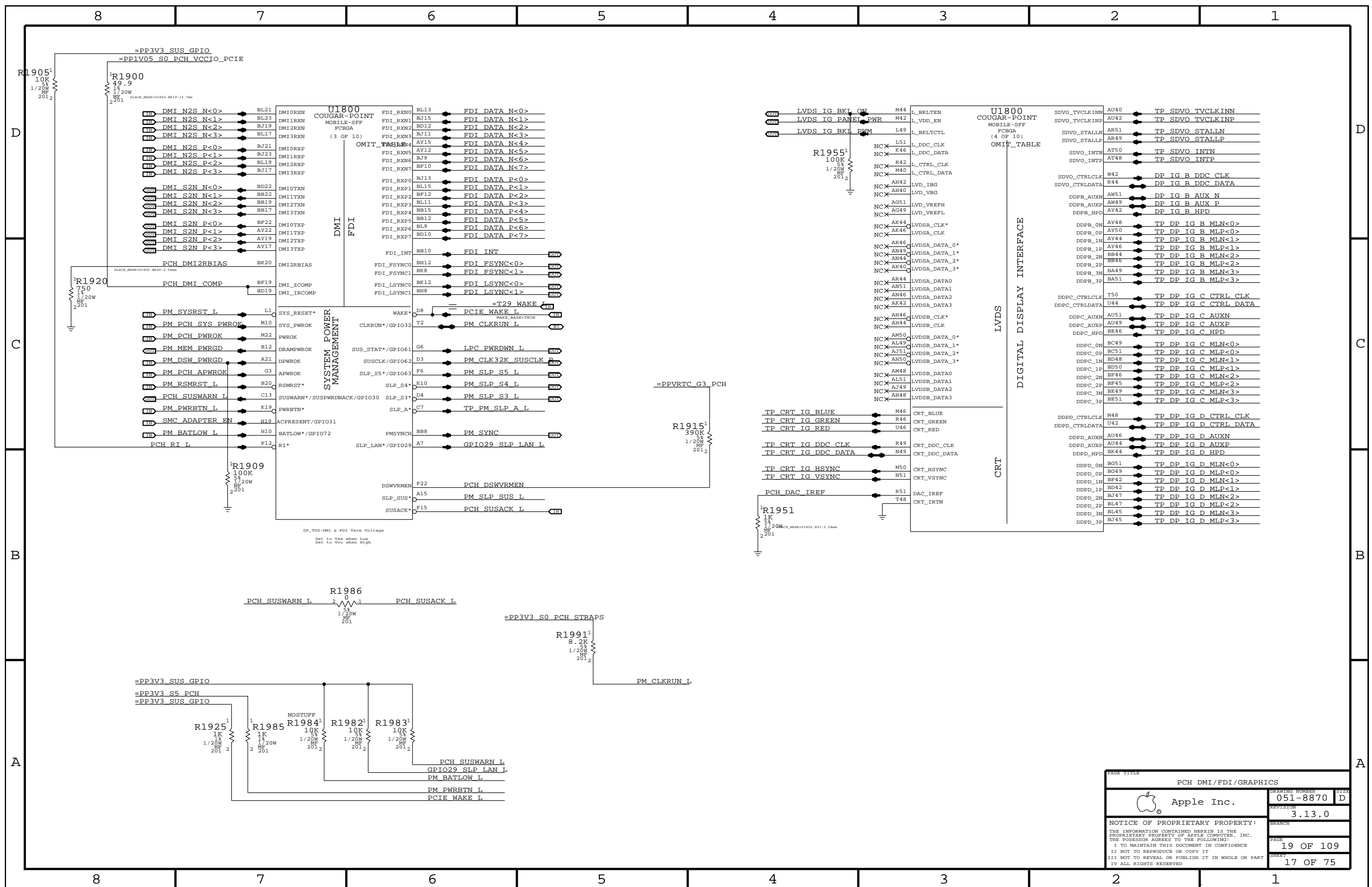






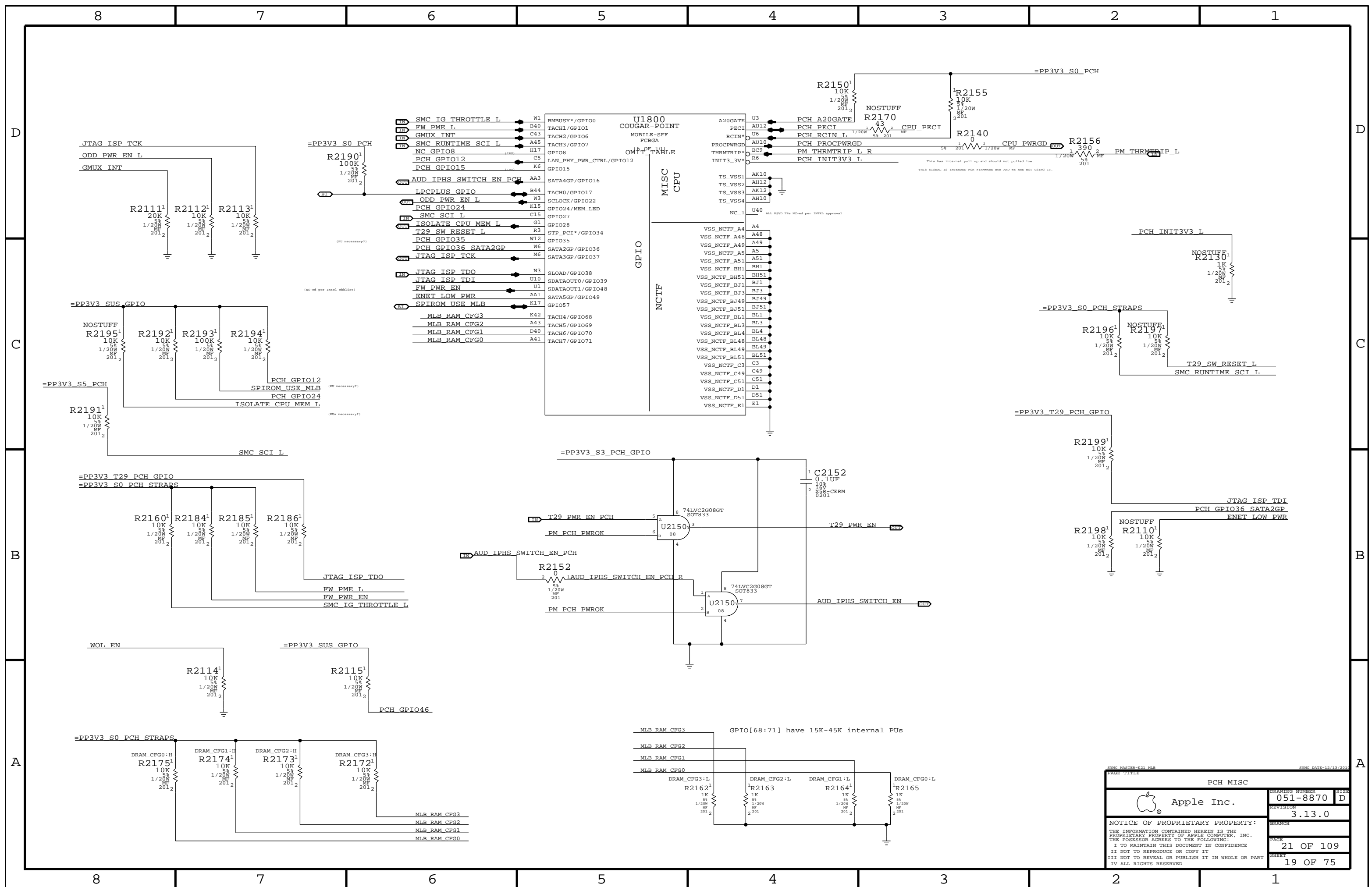




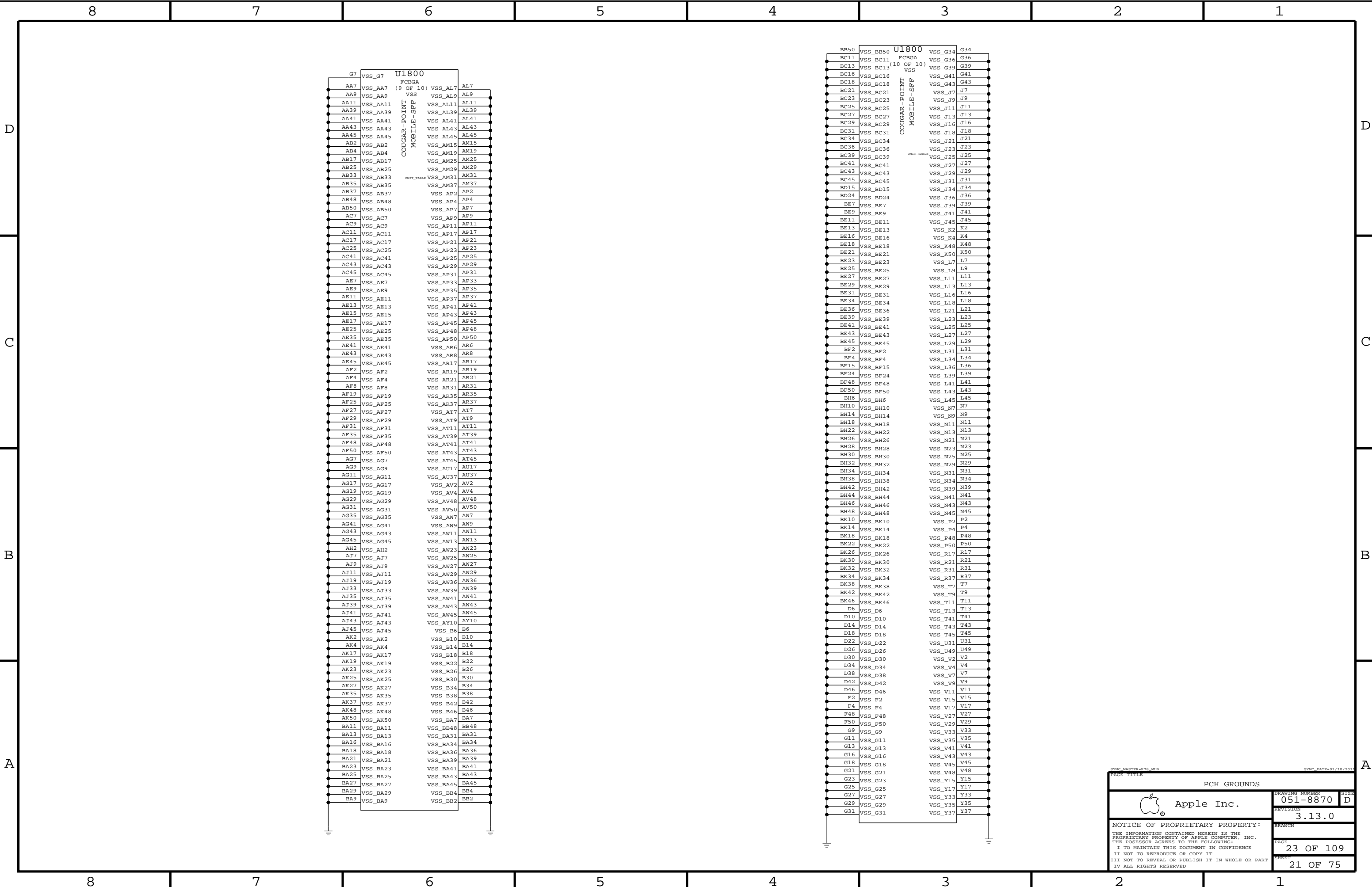













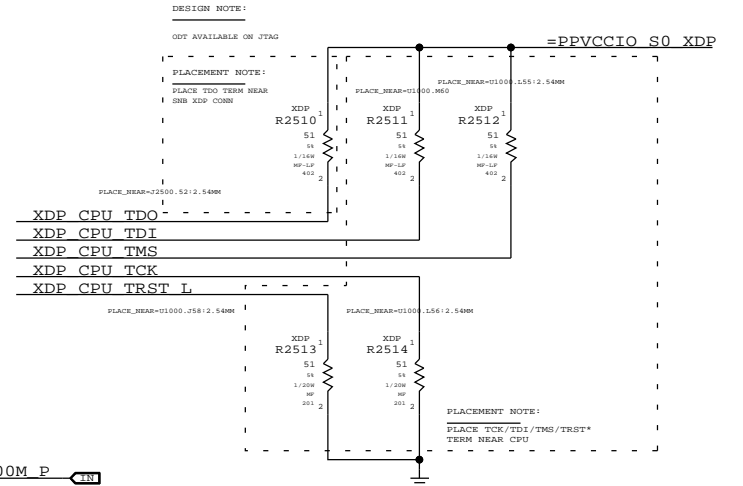
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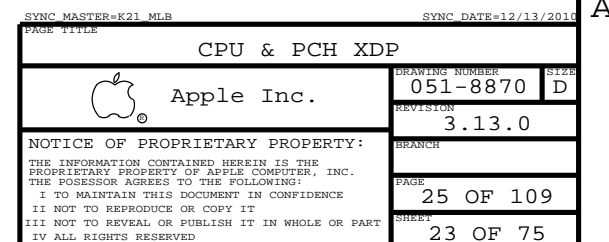
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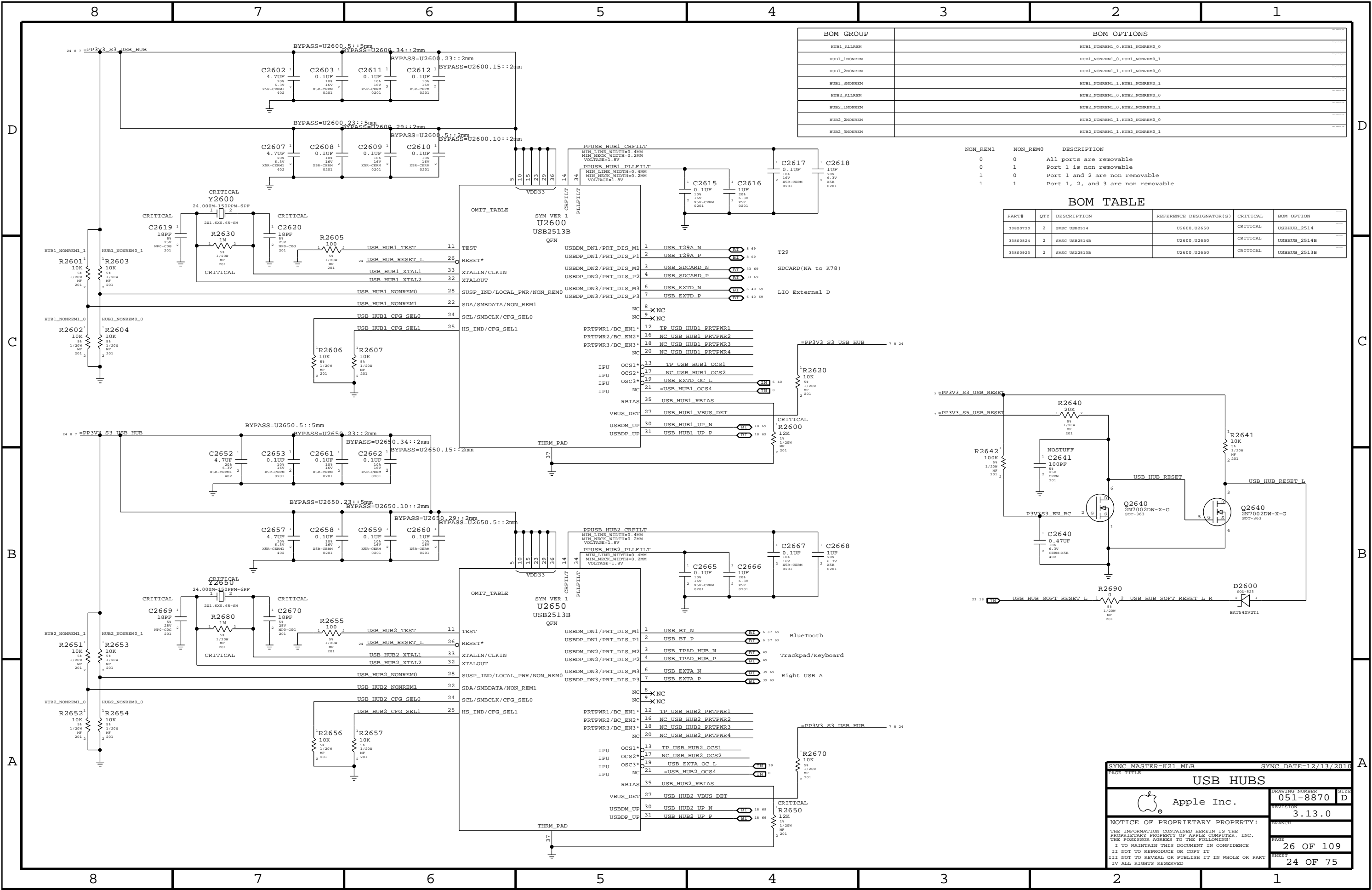
NOTE: This is not the standard XDP pinout  
Use with 920-0782 Adapter Flex to support chipset debug

[illegible]

NOTE: This is not the standard XDP pinout  
Use with 920-0782 Adapter Flex to support chipset debug







BOM GROUP		BOM OPTIONS	
HUB1_ALLREM		HUB1_NONREM0_0	HUB1_NONREM0_0
HUB1_1NONREM		HUB1_NONREM1_0	HUB1_NONREM1_0
HUB1_2NONREM		HUB1_NONREM1_1	HUB1_NONREM1_1
HUB1_3NONREM		HUB1_NONREM1_1	HUB1_NONREM1_1
HUB2_ALLREM		HUB2_NONREM0_0	HUB2_NONREM0_0
HUB2_1NONREM		HUB2_NONREM1_0	HUB2_NONREM1_0
HUB2_2NONREM		HUB2_NONREM1_1	HUB2_NONREM1_1
HUB2_3NONREM		HUB2_NONREM1_1	HUB2_NONREM1_1

NON_REM1	NON_REM0	DESCRIPTION
0	0	All ports are removable
0	1	Port 1 is non removable
1	0	Port 1 and 2 are non removable
1	1	Port 1, 2, and 3 are non removable

BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
33880720	2	SMSC USB2514	U2600,U2650	CRITICAL	USBHUB_2514
33880824	2	SMSC USB2514B	U2600,U2650	CRITICAL	USBHUB_2514B
33880923	2	SMSC UX2513B	U2600,U2650	CRITICAL	USBHUB_2513B

SYNC MASTER=K21 MLB

SYNC DATE=12/13/2010

USB HUBS

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051-8870

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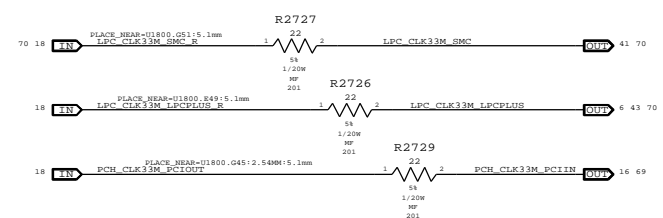
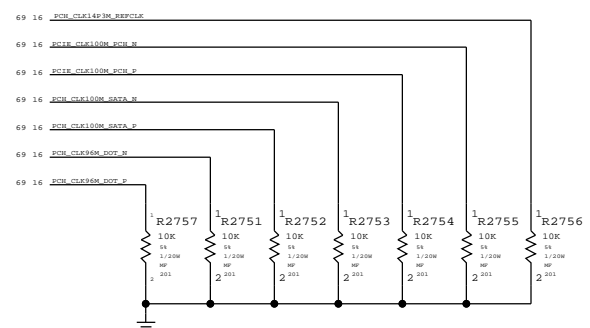
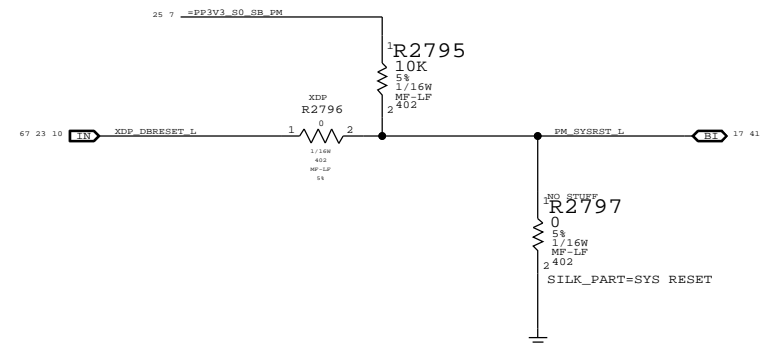
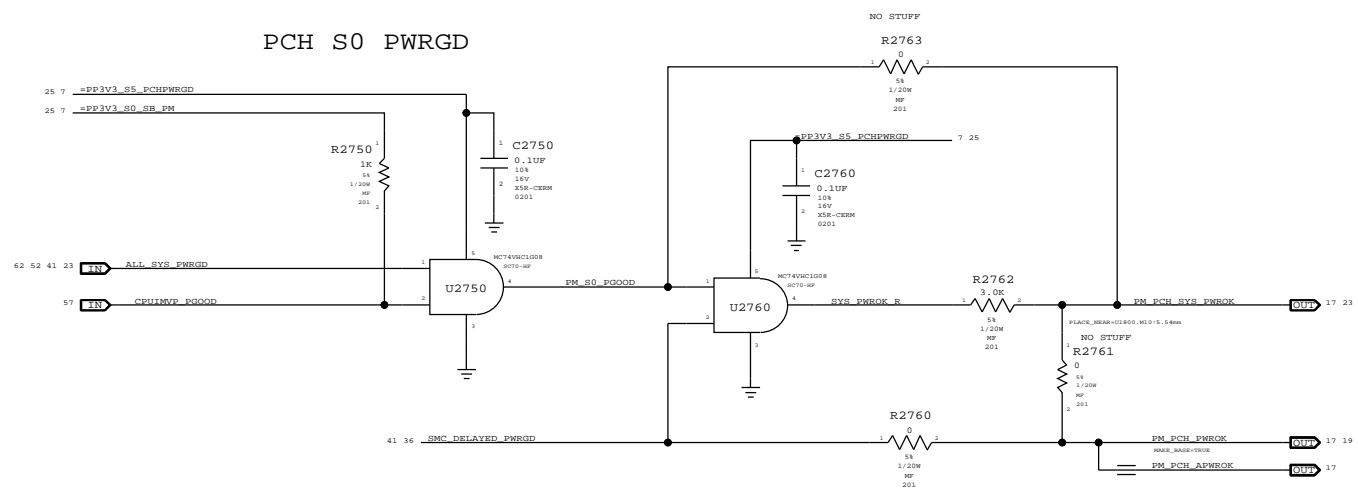
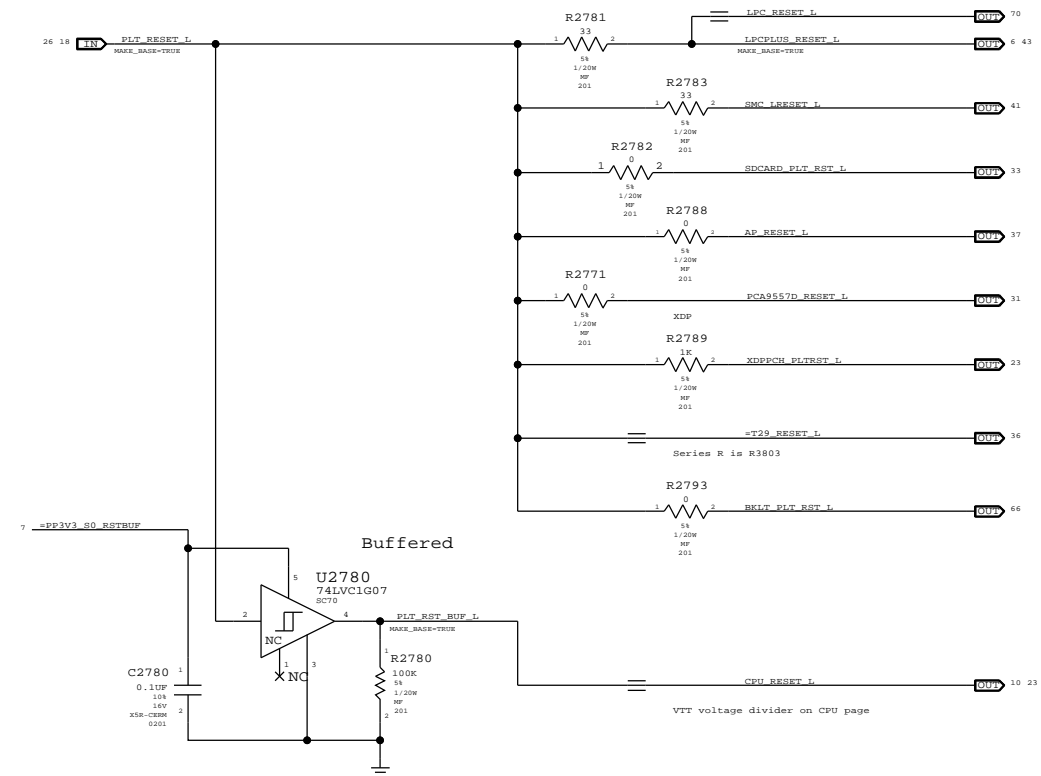
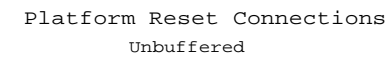
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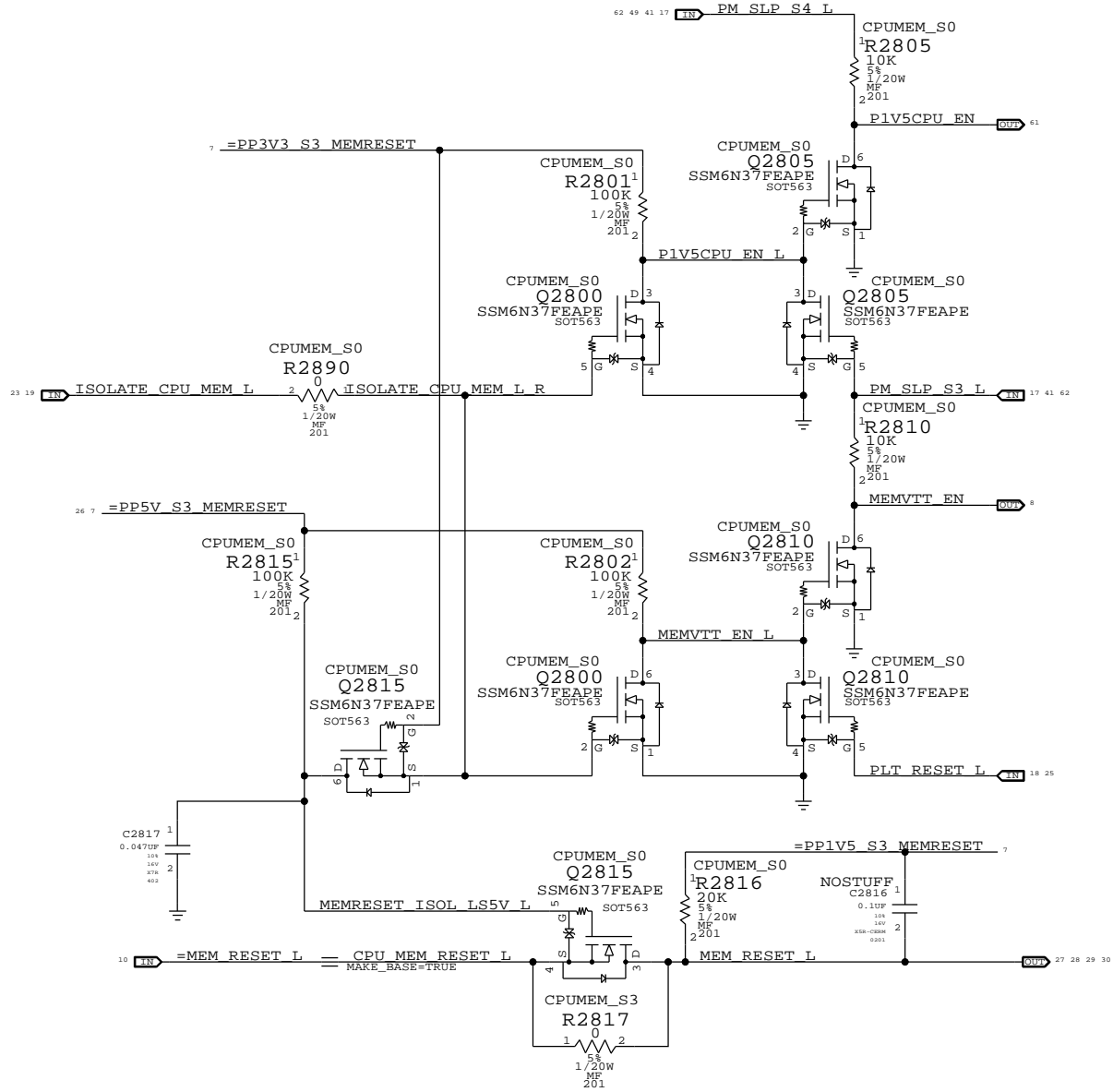


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PAGE TITLE			
Clock (CK505) and Chipset Support			
	Apple Inc.		DRAWING NUMBER <b>051-8870</b>
			SIZE <b>D</b>
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		SHEET <b>25 OF 75</b>	

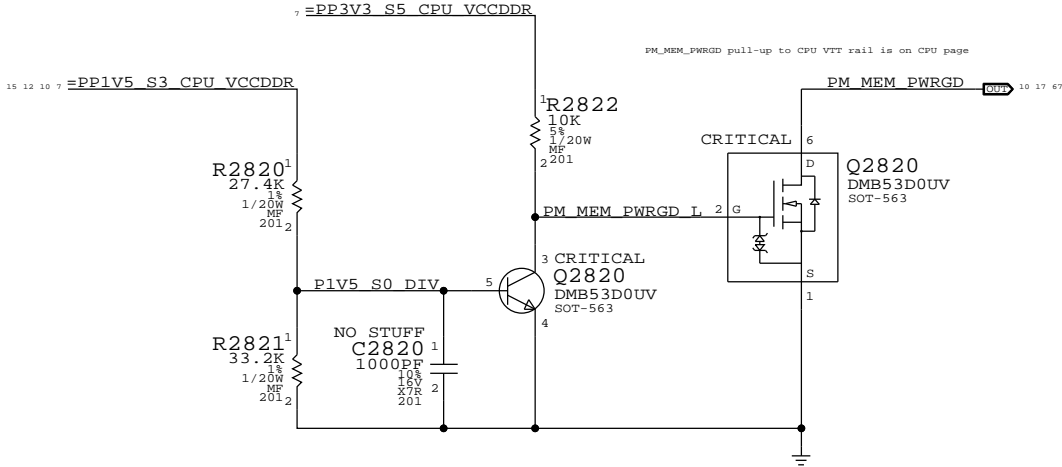
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM\_DRAMRST# output from the S0-DIMMs when necessary.

ISOLATE\_CPU\_MEM\_L GPIO state during S3->S0 transitions determines behavior of signals.  
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM\_RESET\_L not isolated.  
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM\_RESET\_L isolated.

P1V5CPU\_EN = (ISOLATE\_CPU\_MEM\_L + PM\_SLP\_S3\_L) \* PM\_SLP\_S4\_L  
MEMVTT\_EN = (ISOLATE\_CPU\_MEM\_L + PLT\_RST\_L) \* PM\_SLP\_S3\_L  
MEM\_RESET\_L = !ISOLATE\_CPU\_MEM\_L + CPU\_MEM\_RESET\_L

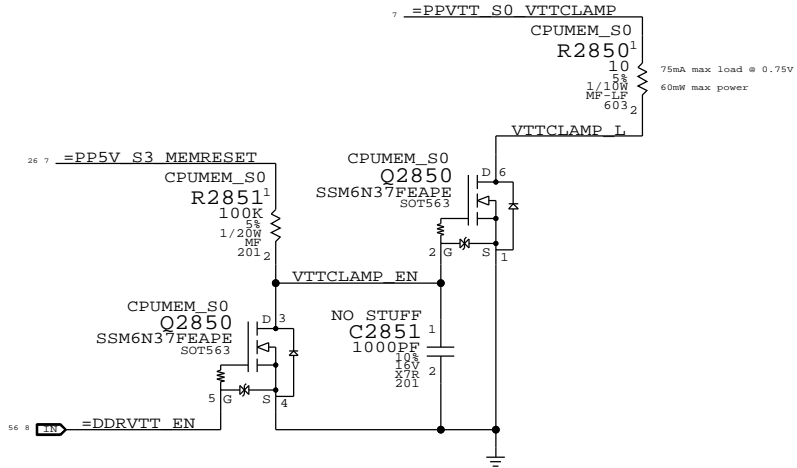


### 1V5 S0 "PGOOD" for CPU



### MEMVTT Clamp

Ensures CKE signals are held low in S3

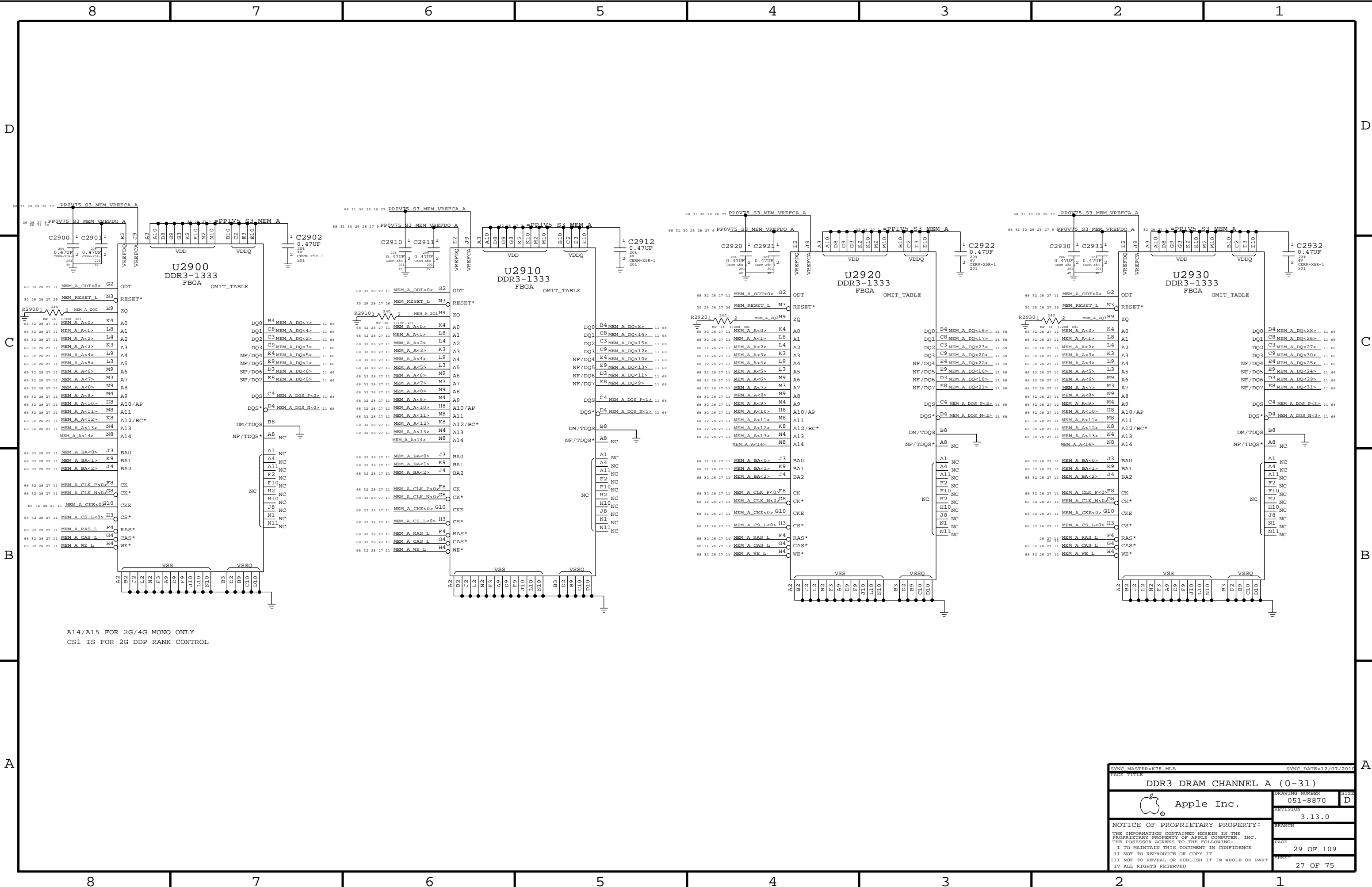


Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	CPU_MEM_RESET_L	1	1
to	1	0	1	1	1	1	1	1
2	0	0	0	1	1	0	0	1
3	0	0	0	1	X	0	0	0
S3	4	0	0	1	X	0	0	1
to	5	0	1	1	0 (*)	1	1	1
6	0	1	1	1	1	1	1	1
S0	7	1	1	1	1	CPU_MEM_RESET_L	1	1


(\*) CPU\_MEM\_RESET\_L asserts due to loss of PM\_MEM\_PWRGD, must wait for software to clear before deasserting ISOLATE\_CPU\_MEM\_L GPIO.

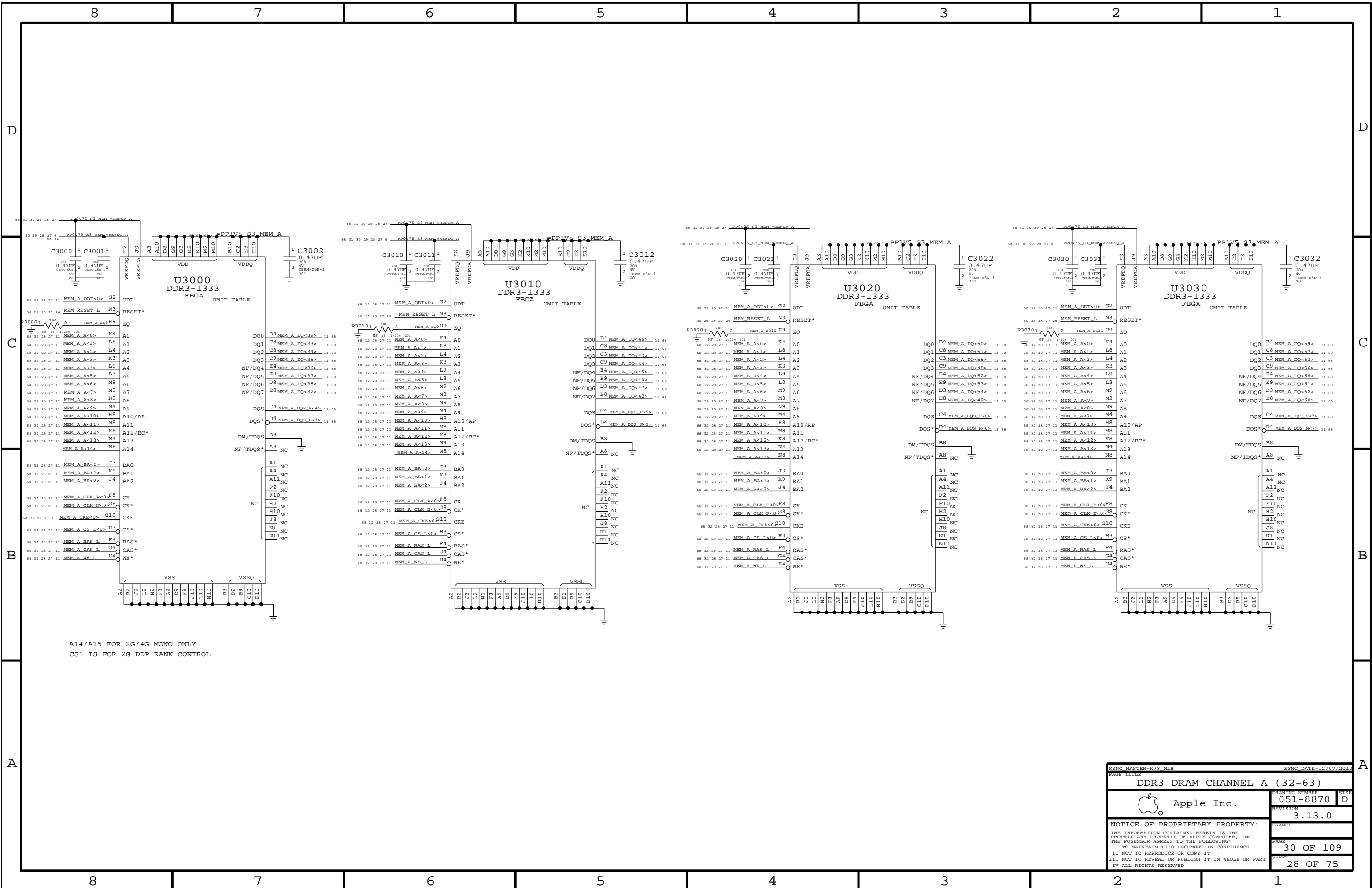
NOTE: In the event of a S3->S5 transition ISOLATE\_CPU\_MEM\_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM\_RESET\_L will not properly assert. Software must deassert ISOLATE\_CPU\_MEM\_L and then generate a valid reset cycle on CPU\_MEM\_RESET\_L.

CPU Memory S3 Support	
Apple Inc.	DRAWING NUMBER 051-8870
REVISION 3.13.0	SIZE D
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PAGE 28 OF 109	SHEET 26 OF 75




A14/A15 FOR 2G/4G MONO ONLY  
CS1 IS FOR 2G DDP RANK CONTROL

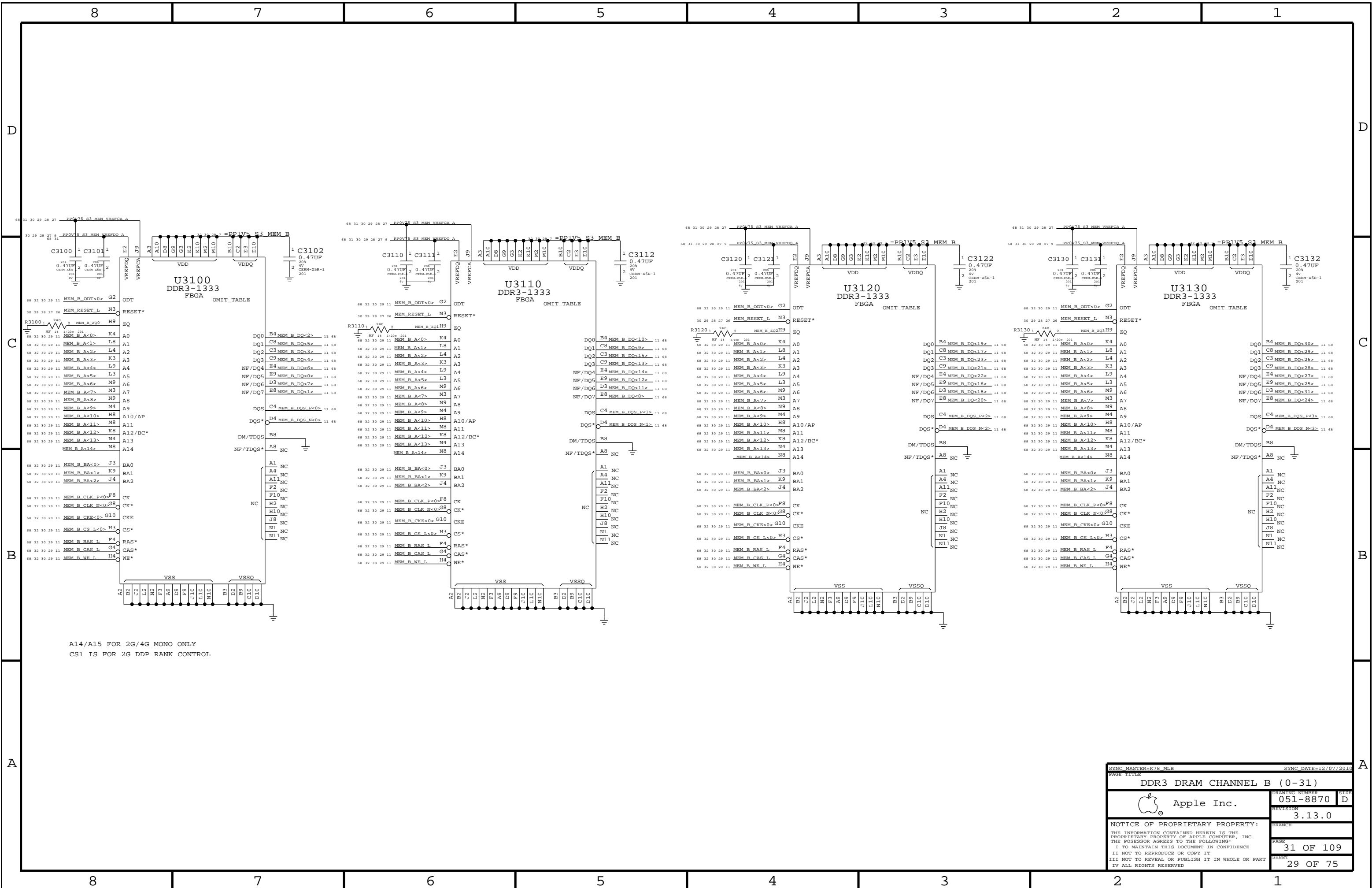
SYNC MASTER=K78 MLB		SYNC DATE=12/07/2010	
PAGE TITLE			
DDR3 DRAM CHANNEL A (0-31)			
 Apple Inc.	DRAWING NUMBER	051-8870	SIZE D
	REVISION	3.13.0	
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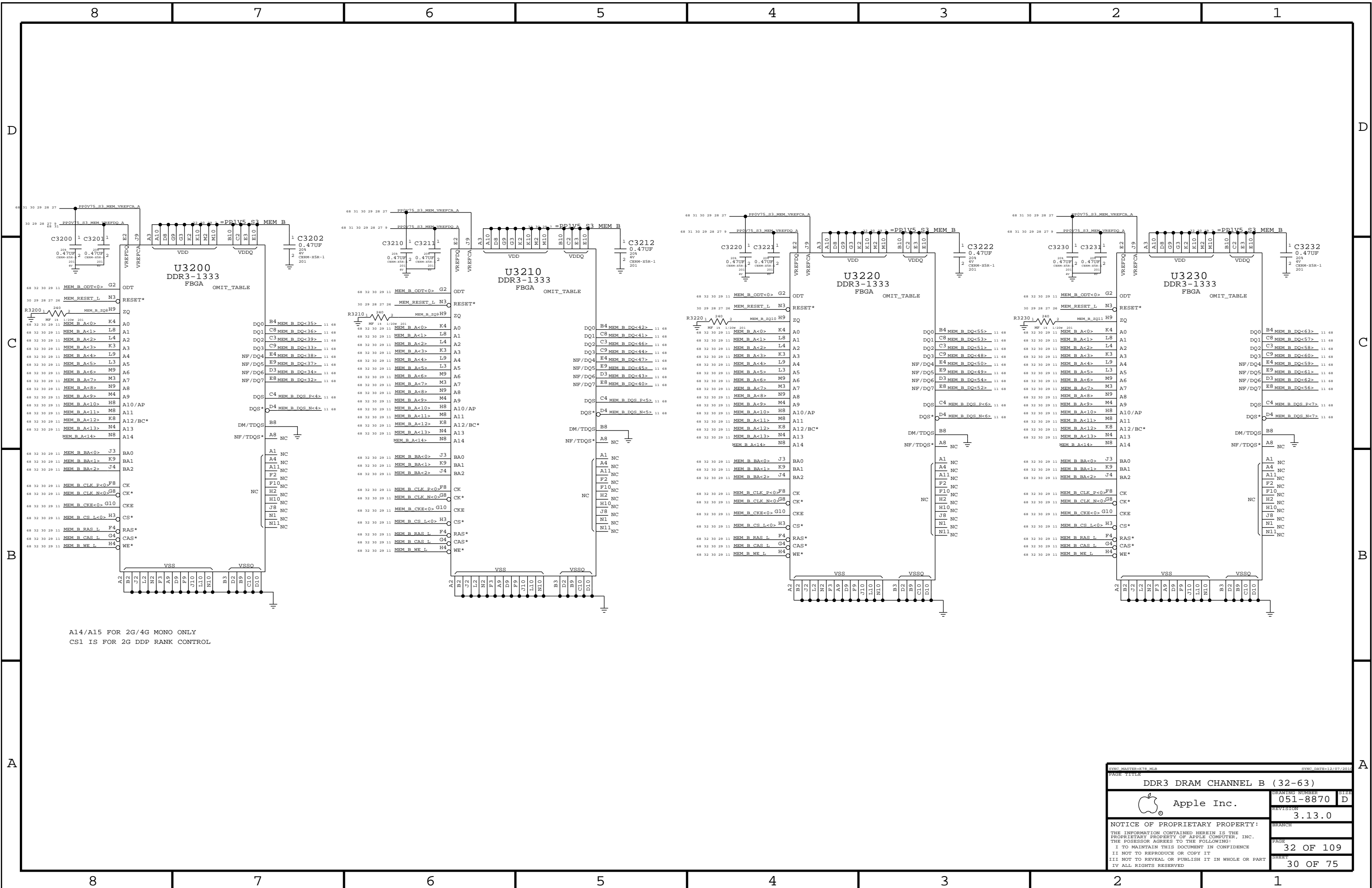


A14/A15 FOR 2G/4G MONO ONLY  
CS1 IS FOR 2G DDP RANK CONTROL


SYNC MASTER=K78 MLB		SYNC DATE=12/07/2010	
PAGE TITLE			
DDR3 DRAM CHANNEL A (32-63)			
 Apple Inc.		DRAWING NUMBER	051-8870
		REVISION	3.13.0
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		PAGE	30 OF 109
		SHEET	28 OF 75







A14/A15 FOR 2G/4G MONO ONLY  
CS1 IS FOR 2G DDP RANK CONTROL

SYMC MASTER=S78 MLR		SYMC DATE=12/07/2011	
PAGE TITLE			
DDR3 DRAM CHANNEL B		(32-63)	
	Apple Inc.	DRAWING NUMBER	051-8870
		SIZE	D
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		BRANCH	
		PAGE	32 OF 109
		SHEET	30 OF 75

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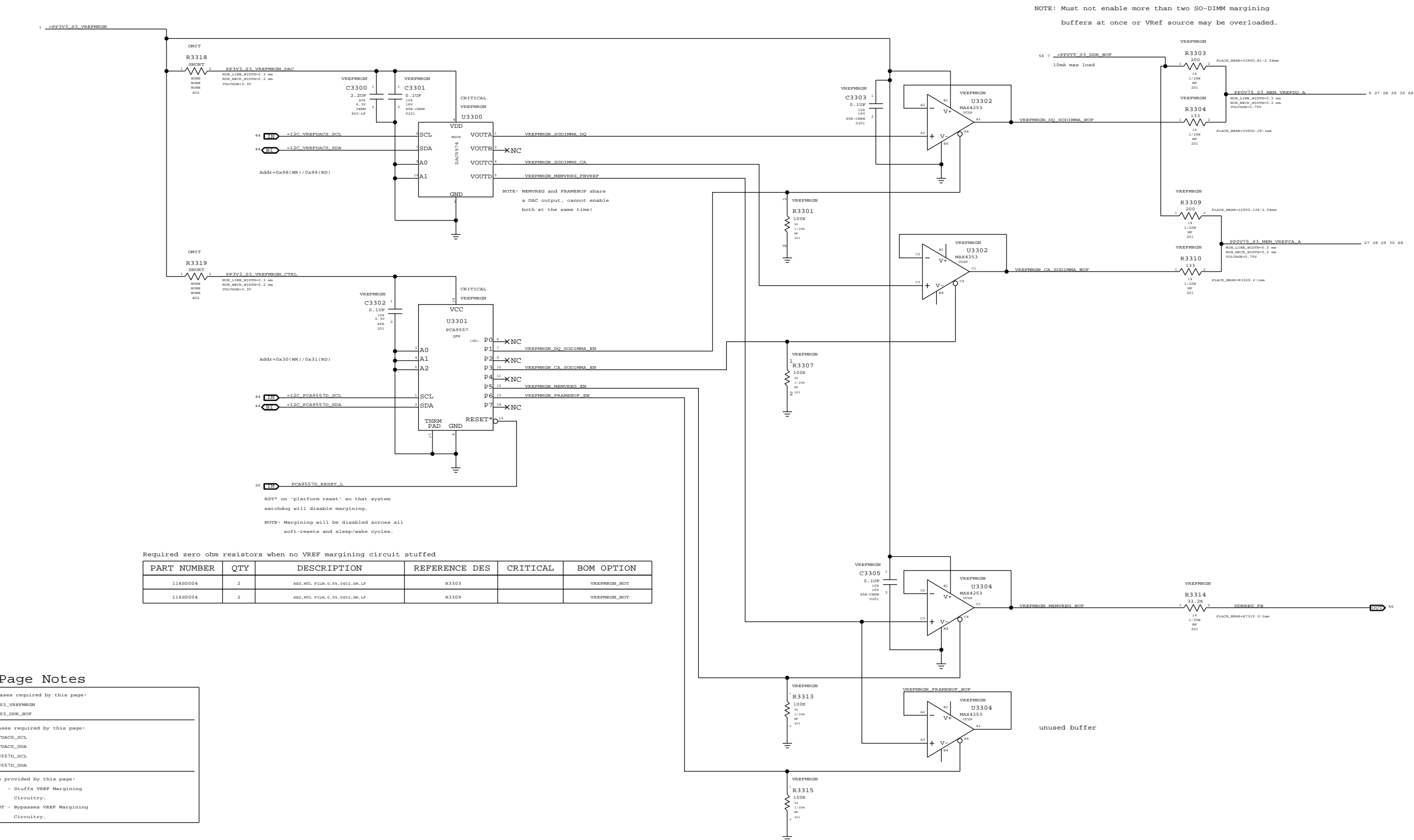
A

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Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES_MTL FILM,0.5%,0402,SM,LF	R3303		VREFMGN_NOT
116S0004	2	RES_MTL FILM,0.5%,0402,SM,LF	R3309		VREFMGN_NOT

Page Notes

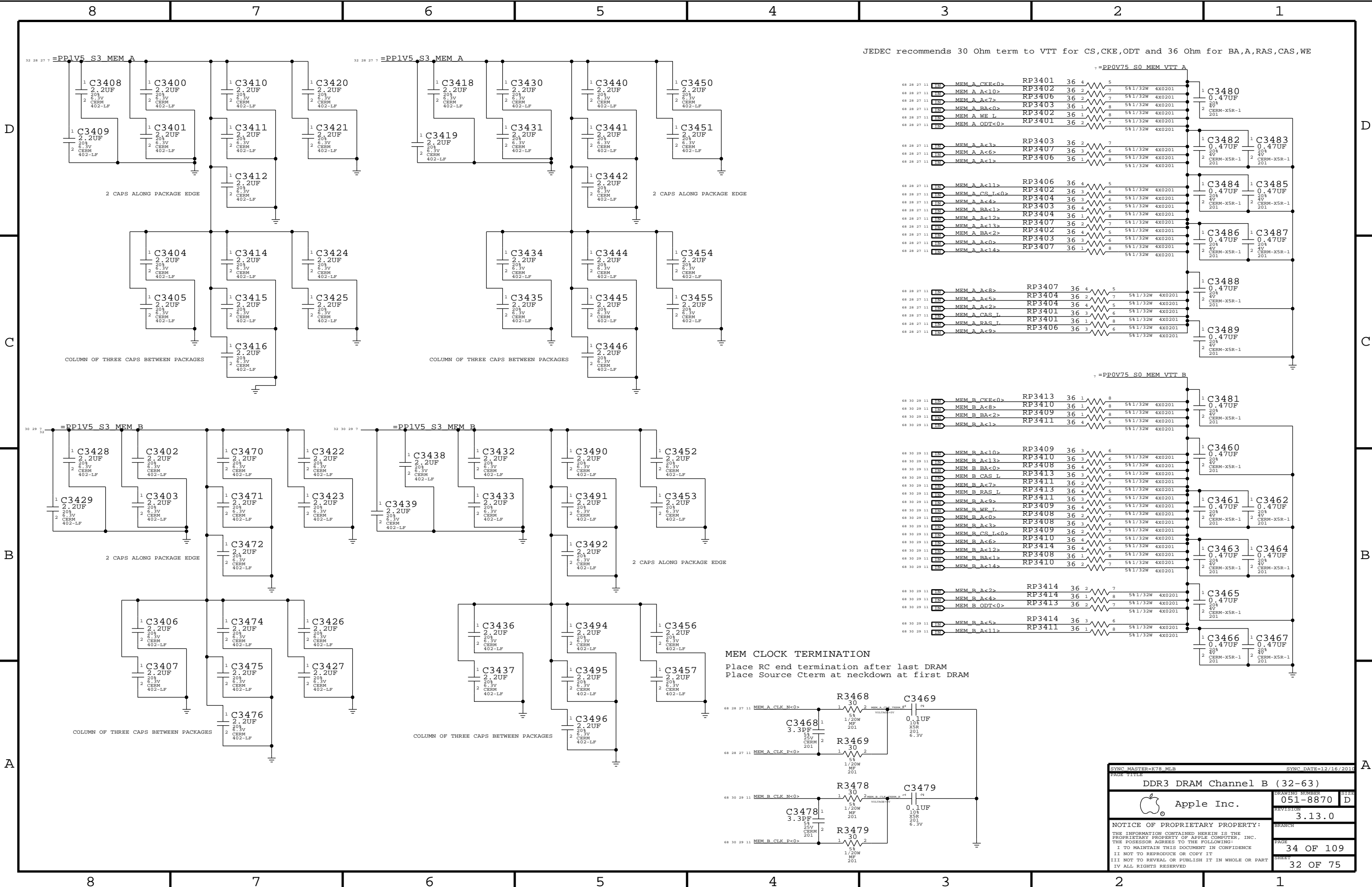
Power aliases required by this page:  
- =PP3V3\_S3\_VREFMGN  
- =PPVTT\_S3\_DDR\_BUF

Signal aliases required by this page:  
- =I2C\_VREFDACS\_SCL  
- =I2C\_VREFDACS\_SDA  
- =I2C\_PCA9557D\_SCL  
- =I2C\_PCA9557D\_SDA

BOM options provided by this page:  
VREFMGN - Stuffs VREF Margining Circuitry.  
VREFMGN\_NOT - Bypasses VREF Margining Circuitry.

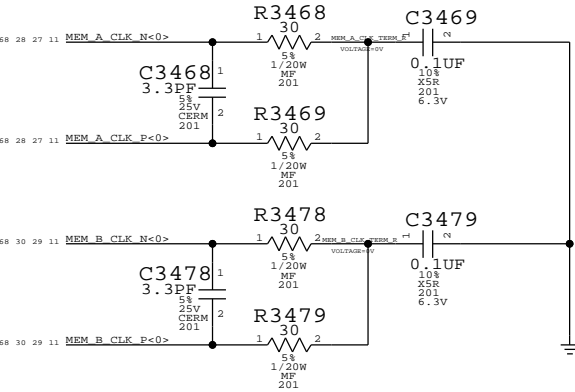
	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% Vref)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4		
Nominal value		0.75V (DAC: 0x3A)			1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:		0.300V - 1.200V (+/- 450mV)			1.998V - 1.002V (+/- 498mV)	1.056V - 1.442V (+/- 180mV)
DAC range:		0.000V - 1.501V (0x00 - 0x74)			0.000V - 1.501V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
VRef current:		+3.4mA - -3.4mA (- = sourced)			+33uA - -33uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:		7.69mV / step @ output			8.59mV / step @ output	1.51mV / step @ output


PAGE TITLE		SYMC DATE=01/10/2011	
FSB/DDR3/FRAMBUF Vref Margining			
DRAWING NUMBER		051-8870	SIZE D
REVISION		3.13.0	
BRANCH			
PAGE		33 OF 109	
SHEET		31 OF 75	
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JEDEC recommends 30 Ohm term to VTT for CS,CKE,ODT and 36 Ohm for BA,A,RAS,CAS,WE

MEM CLOCK TERMINATION  
Place RC end termination after last DRAM  
Place Source Cterm at neckdown at first DRAM



SYNC MASTER=K78 MLB		SYNC DATE=12/16/2010	
PAGE TITLE			
DDR3 DRAM Channel B (32-63)			
 Apple Inc.		DRAWING NUMBER	SHEET
		051-8870	D
		REVISION	
		3.13.0	
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		BRANCH	
		PAGE	34 OF 109
		SHEET	32 OF 75







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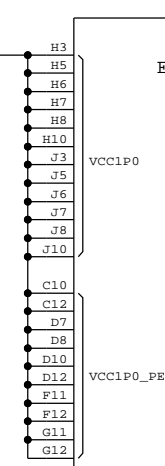
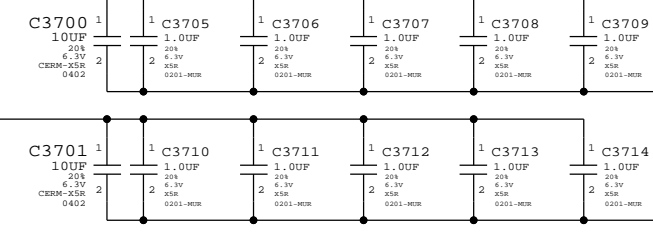
D

C

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A

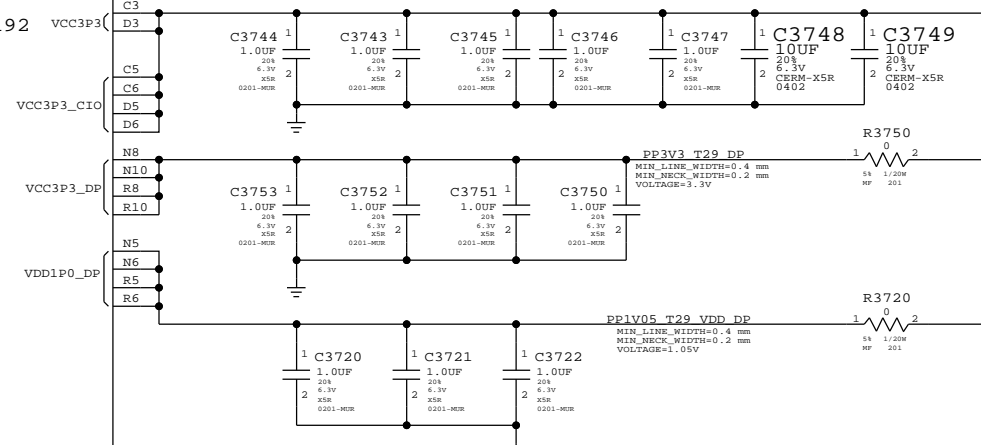
35 7 =PP1V05 T29\_RTR  
2100 mA (Single Port)  
2250 mA (Dual Port)  
EDP: 3000 mA



CRITICAL  
OMIT\_TABLE  
U3600  
EAGLE\_RIDGE-192  
FCBGA  
(2 OF 2)

VCC

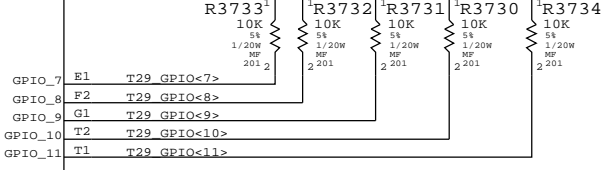
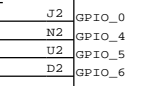
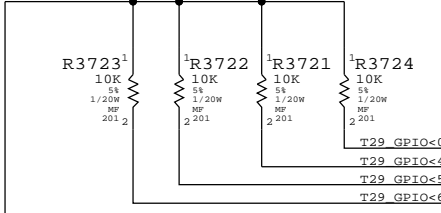
GND




=PP3V3 T29\_RTR  
135 mA (Single-Port)  
152 mA (Dual-Port)  
EDP: 200 mA

0-ohms are placeholders for now, replace with proper values after characterization.

=PP1V05 T29\_RTR 7 35  
2100 mA (Single Port)  
2250 mA (Dual Port)  
EDP: 3000 mA



SYNC MASTER=K75 MLB		SYNC DATE=01/10/2011	
PAGE TITLE			
T29 Host (2 of 2)			
 Apple Inc.	DRAWING NUMBER	051-8870	SIZE D
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PAGE		37 OF 109	
SHEET		35 OF 75	

## Page Notes

Power aliases required by this page:

- PPVIN\_SW\_T29BST (8-13V Boost Input)
- PP18V\_T29\_REG (18V Boost Output)
- PP3V3\_T29\_P3V3T29FET (3.3V FET Input)
- PP3V3\_T29\_FET (3.3V FET Output)
- PP3V3\_S0\_T29PWRCTL
- PP1V05\_T29\_P1V05T29FET (1.05V FET Input)
- PP1V05\_T29\_FET (1.05V FET Output)

Signal aliases required by this page:

- T29\_CLKREQ\_L
- T29\_RESET\_L

BOM options provided by this page:

T29BST:Y - Stuffs 18V boost circuitry.

## T29 18V Boost Regulator

SI8409DB:  
Vds(max): -30V  
Vgs(max): +/-12V  
Vgs(th): -1.4V  
Rds(on): 46mOhm @ 4.5V Vgs  
Id(max): 3.7A @ 70C

CRITICAL  
T29BST:Y  
Q3880  
SI8409DB  
BGA

CRITICAL  
T29BST:Y  
L3895  
6.8UH-4.0A  
PIMB062D-SM

CRITICAL  
T29BST:Y  
D3895  
POWER01-123  
DFLS230L

D

D

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C

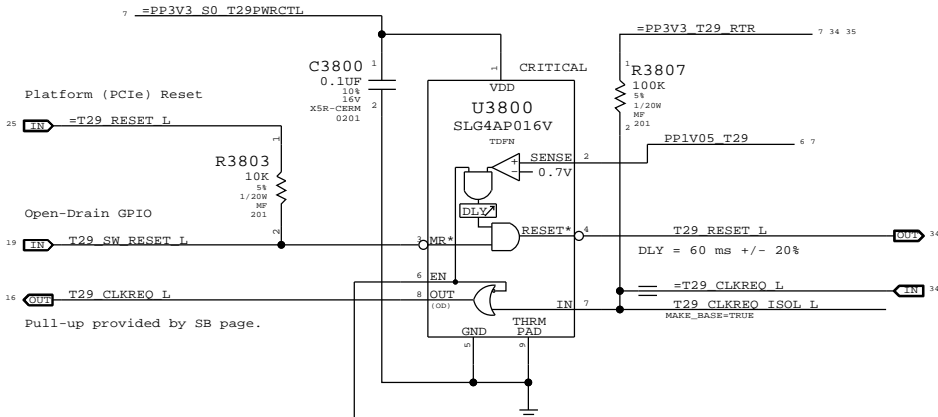
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B

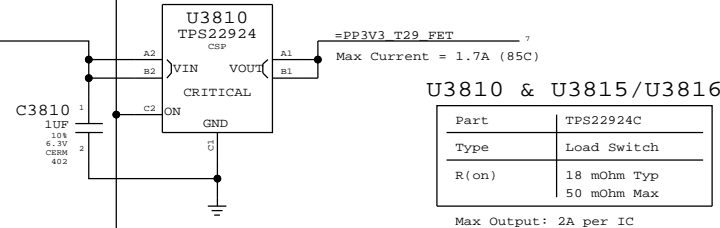
A

A

### Supervisor & CLKREQ# Isolation



### 3.3V T29 Switch

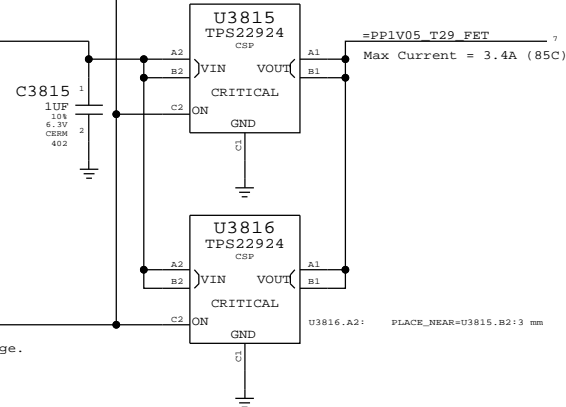


### U3810 & U3815/U3816

Part	TPS22924C
Type	Load Switch
R(on)	18 mOhm Typ 50 mOhm Max


Max Output: 2A per IC

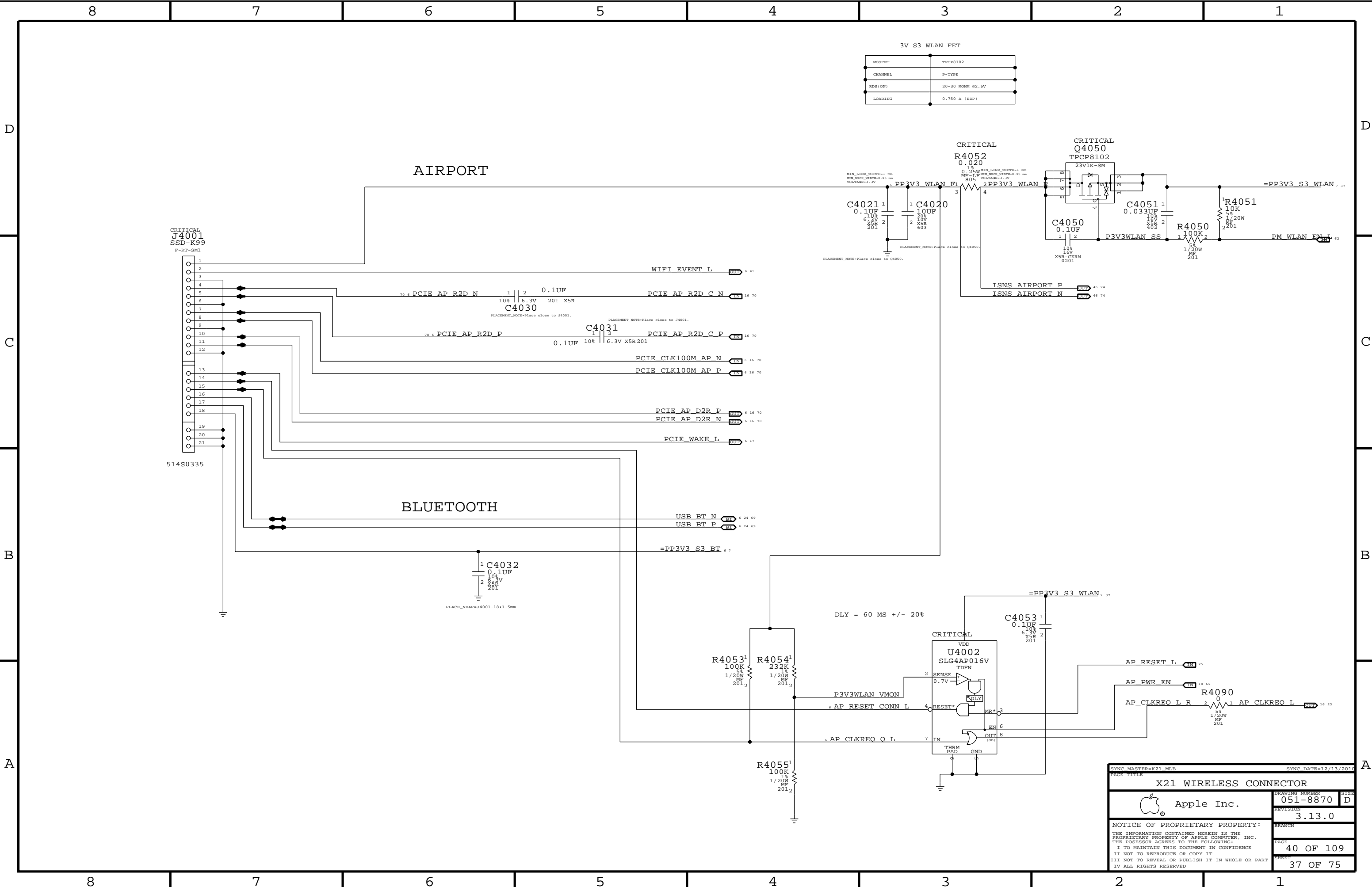
### 1.05V T29 Switch




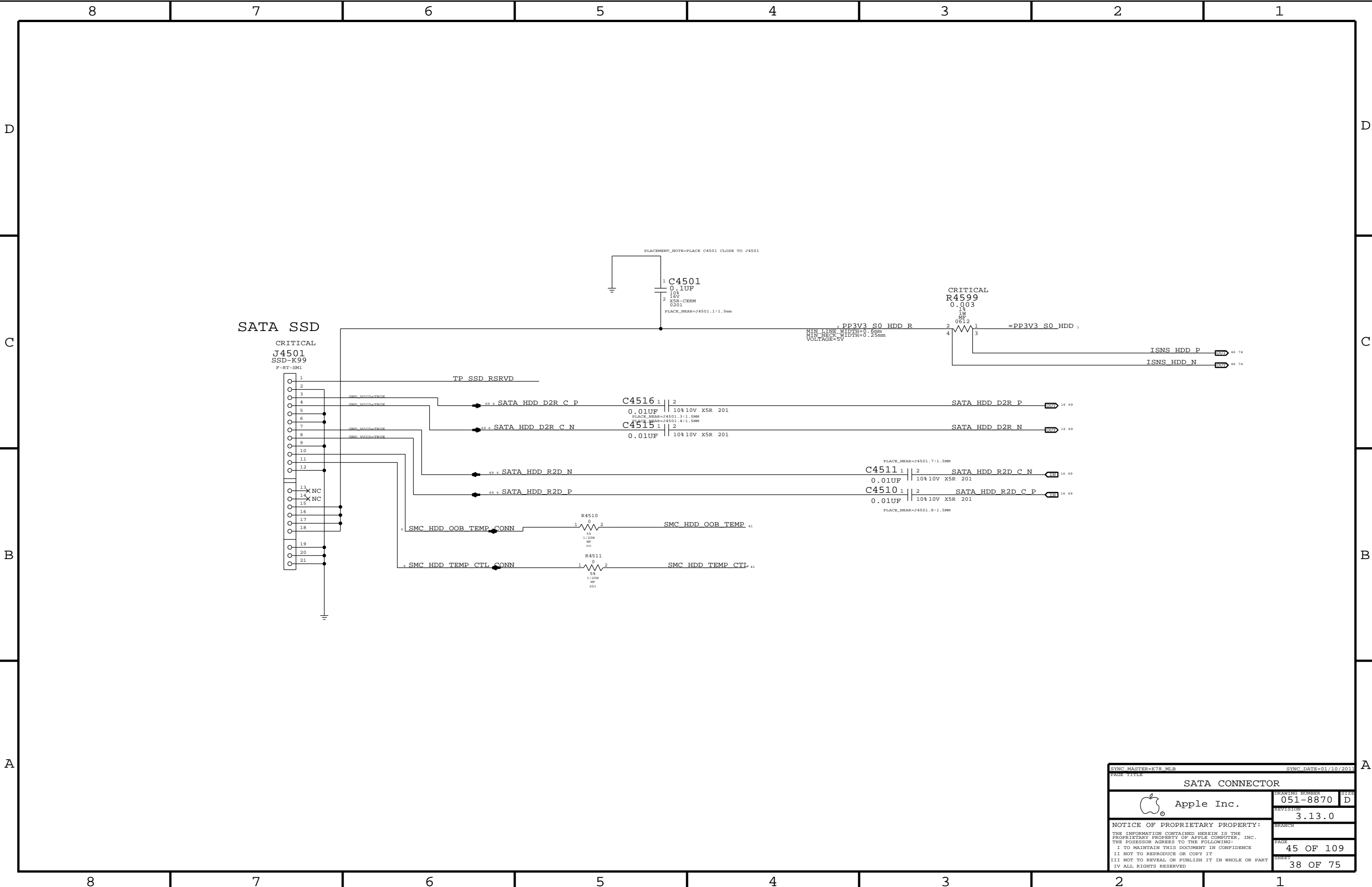
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SYNC MASTER=K75 MLB		SYNC DATE=01/10/2013	
PAGE TITLE			
T29 Power Support			
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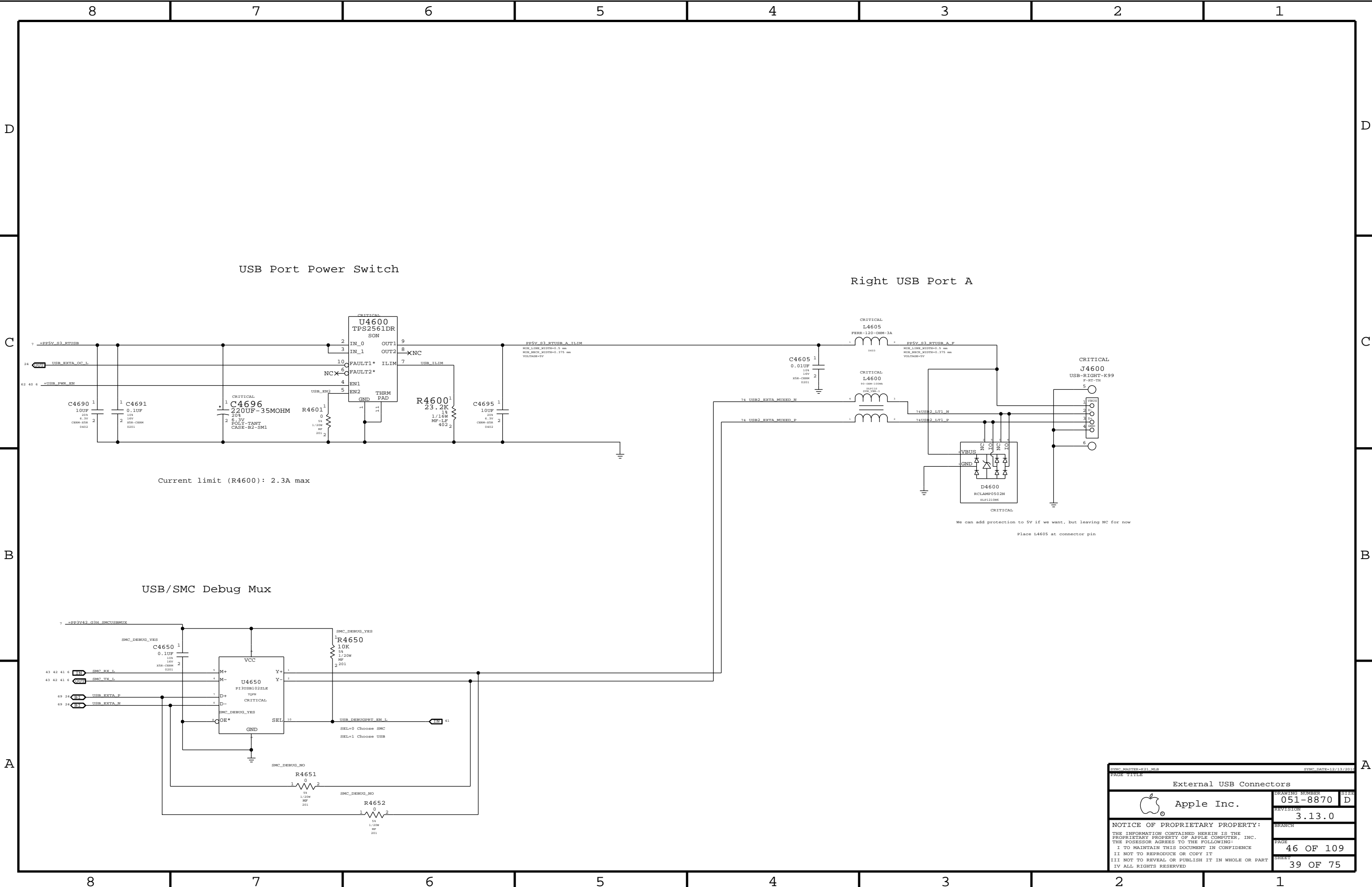


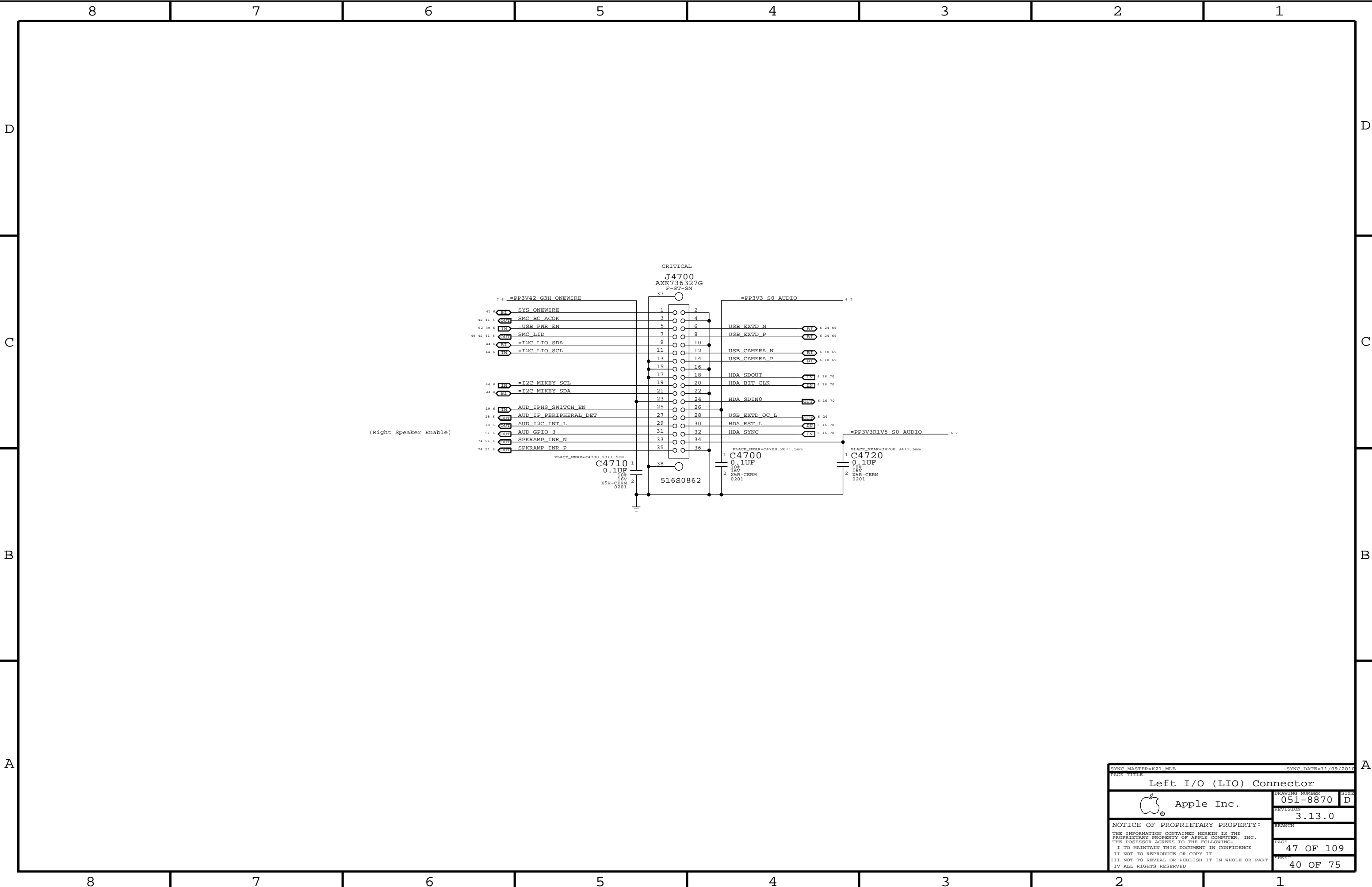
SYNC MASTER=X21 MLB		SYNC DATE=12/13/2010	
PAGE TITLE			
X21 WIRELESS CONNECTOR			
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		SIZE	D
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		BRANCH	
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SYNC MASTER=K78 MLB		SYNC DATE=01/10/2013	
PAGE TITLE			
SATA CONNECTOR			
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SYNC MASTER=K21 MLB

SYNC DATE=11/09/2010

Left I/O (LIO) Connector

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051-8870

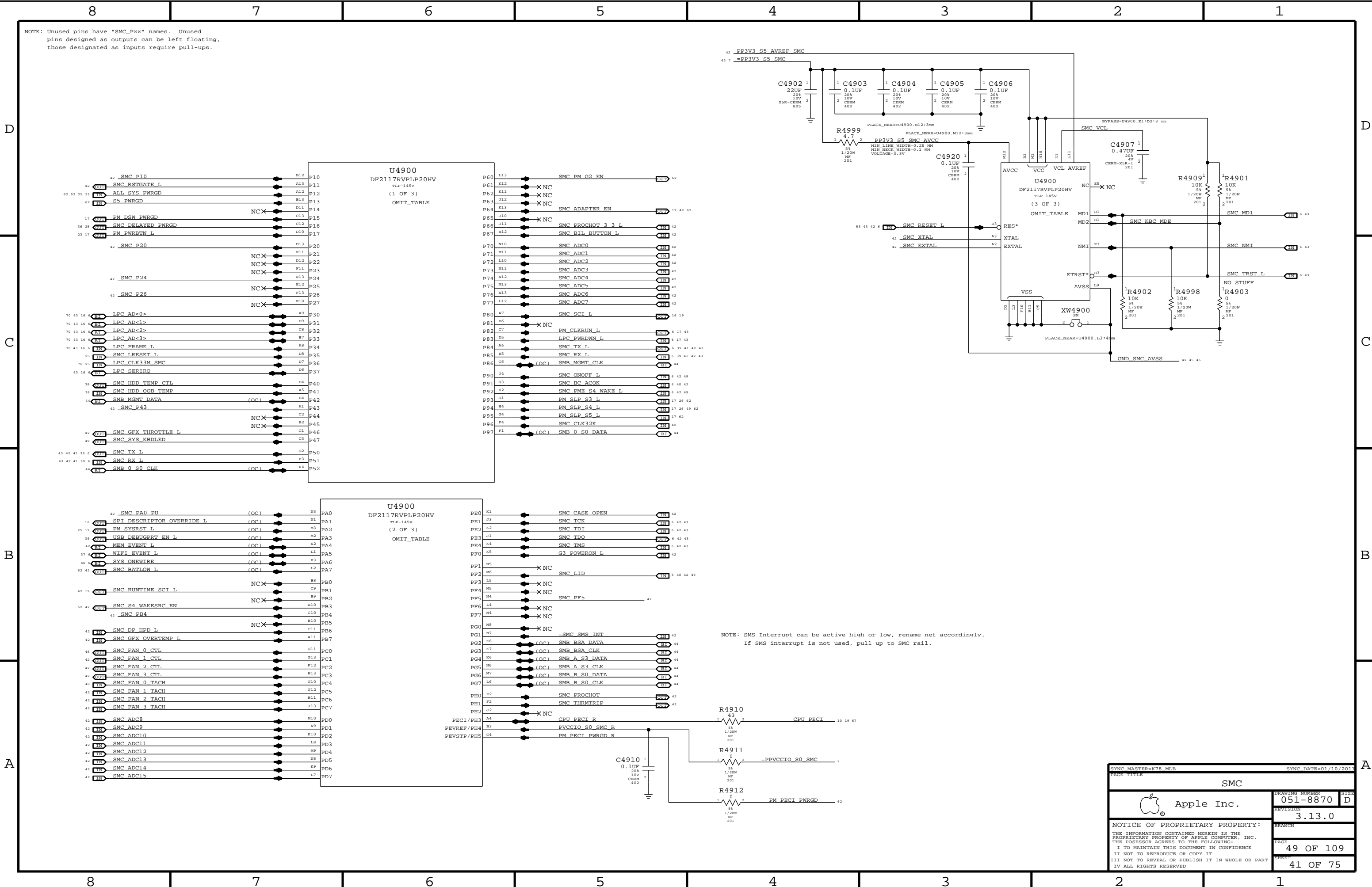
REVISION  
3.13.0

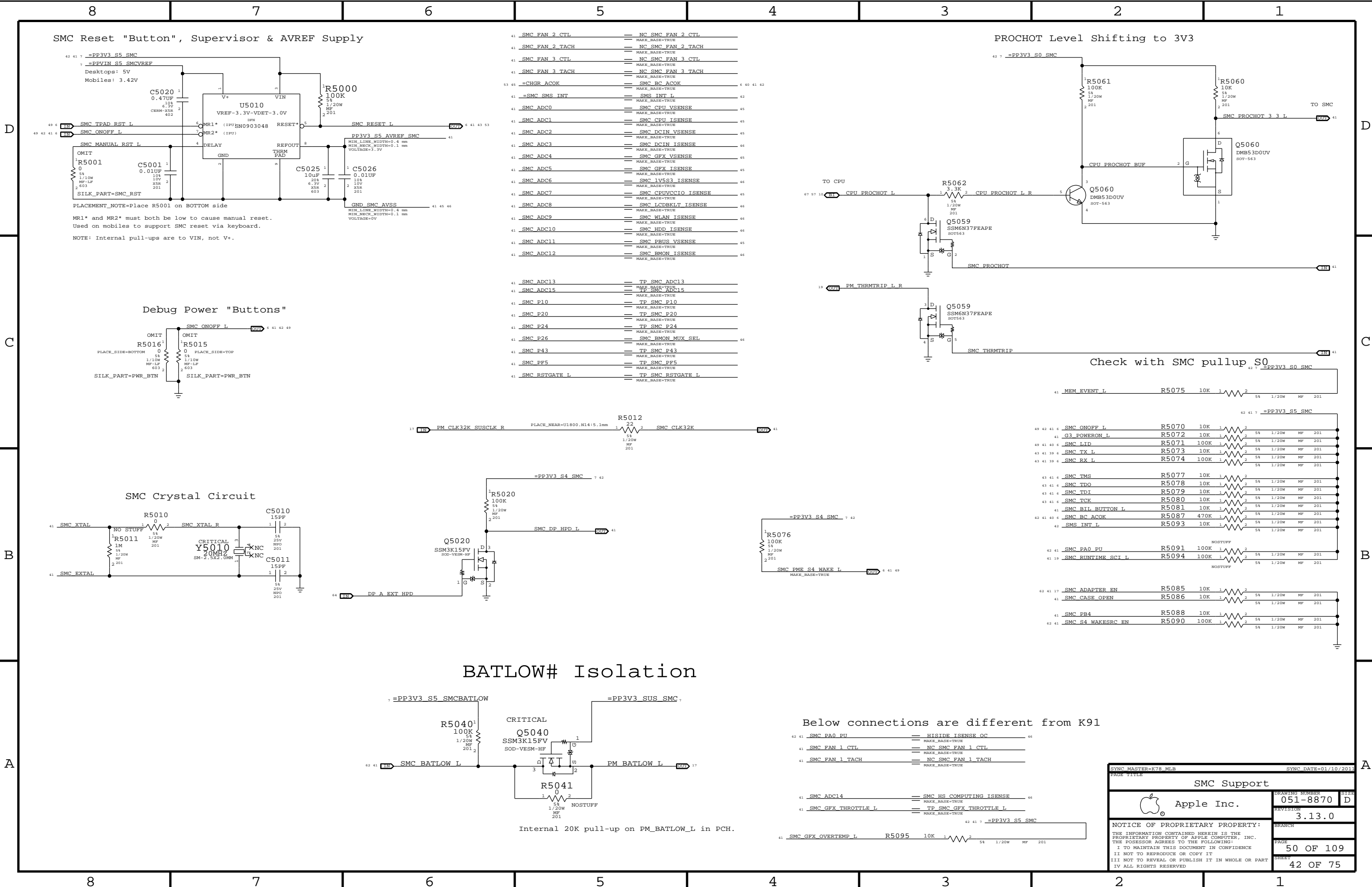
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PAGE  
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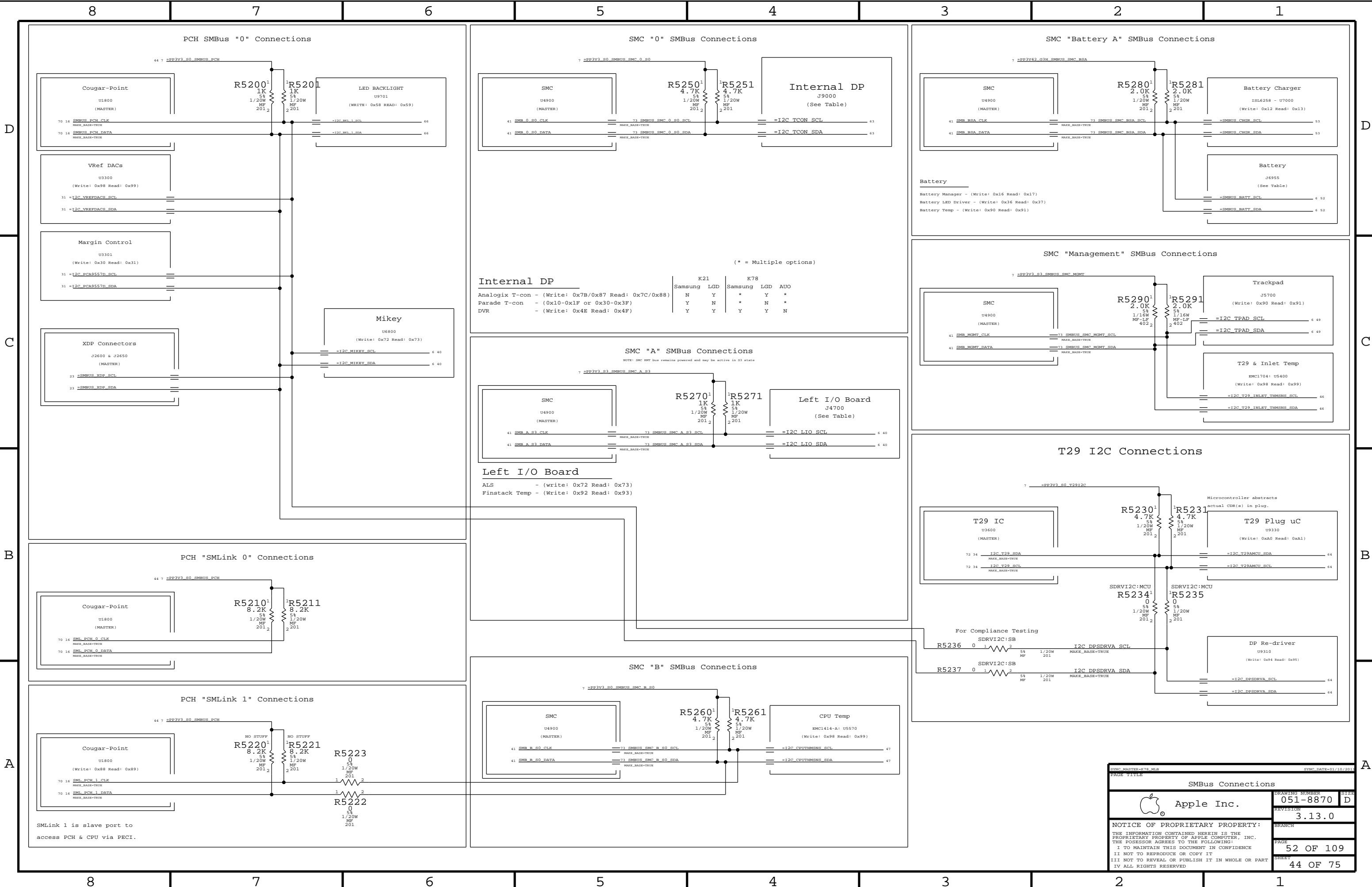
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## C

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SYMC PARTNERSHIP WEB

SYMC DATE=01/10/2011

Apple Inc.

051-8870

3.13.0

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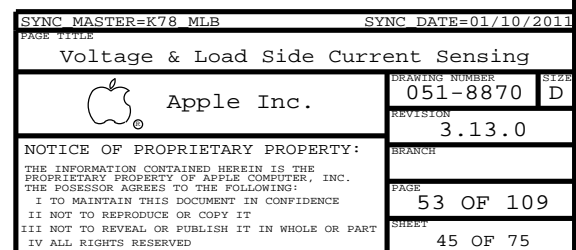


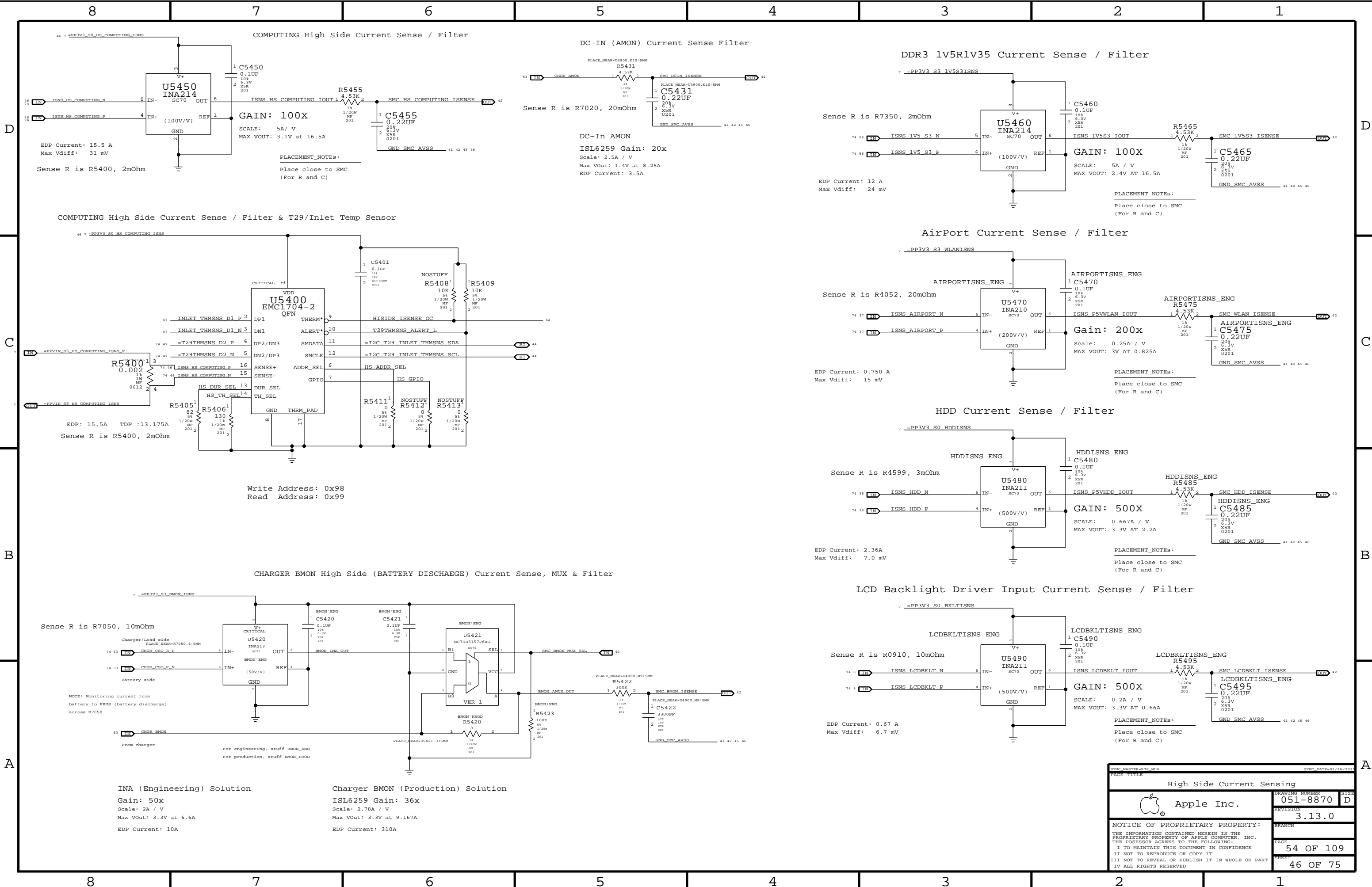
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## 4 59 5

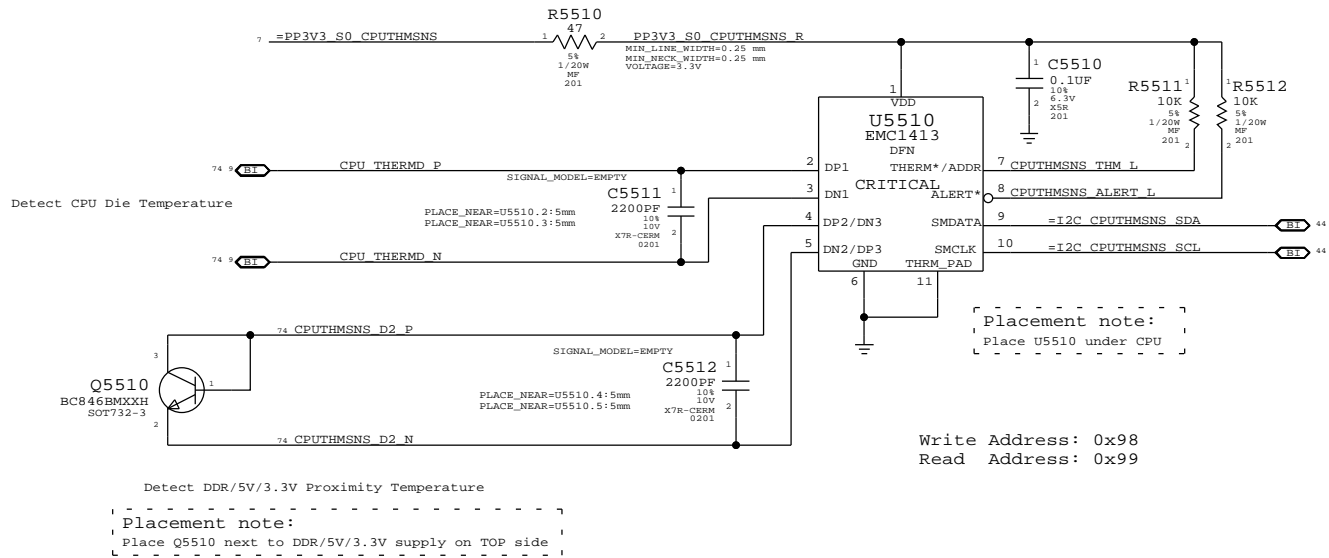
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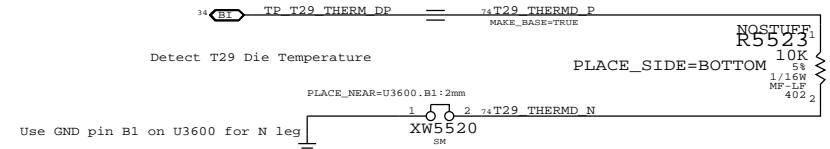


PAGE TITLE		PAGE TITLE	
High Side Current Sensing		High Side Current Sensing	
Apple Inc.		DRAWING NUMBER	051-8870
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CPU Proximity Sensor



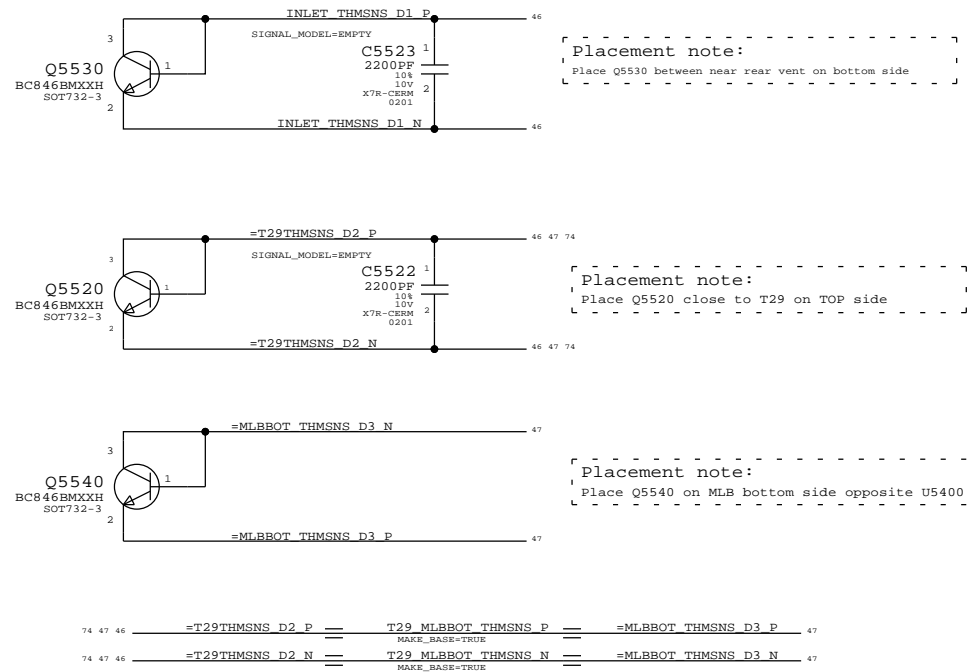
T29 Die




PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MP,1/20W,100K OHM,5,0201,0ND	C5361		VCCIOISNS_PROD
117S0008	1	RES,MP,1/20W,100K OHM,5,0201,0ND	C5475		AIRPORTISNS_PROD
117S0008	1	RES,MP,1/20W,100K OHM,5,0201,0ND	C5485		HDDISNS_PROD
117S0008	1	RES,MP,1/20W,100K OHM,5,0201,0ND	C5495		LCDBKLTISNS_PROD

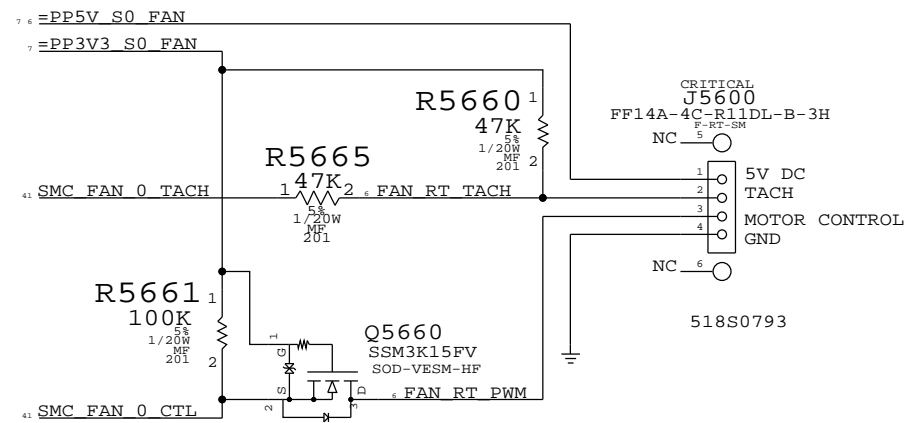
Replacing caps with 100K PD on ISENSE SMC inputs


T29,MLB Bottom & Inlet Proximity Sensors



SYNC MASTER=K75 MLB		SYNC DATE=01/16/2013	
PAGE TITLE			
Thermal Sensors			
 Apple Inc.		DRAWING NUMBER	051-8870
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FAN CONNECTOR



SYNC MASTER=K75 MLB		SYNC DATE=01/10/2011	
PAGE TITLE			
Fan			
	Apple Inc.	DRAWING NUMBER	051-8870
		SIZE	D
		REVISION	3.13.0
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		PAGE	56 OF 109
		SHEET	48 OF 75



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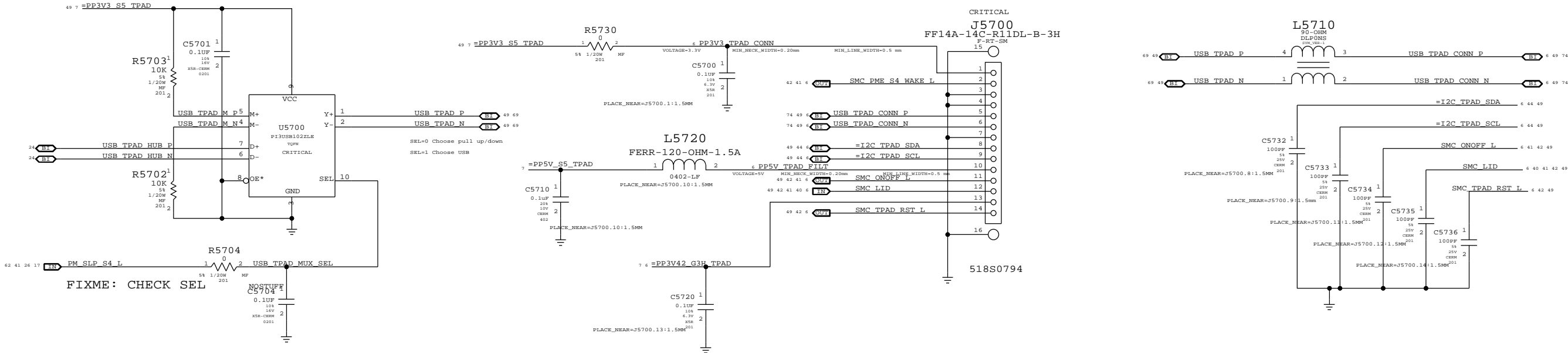
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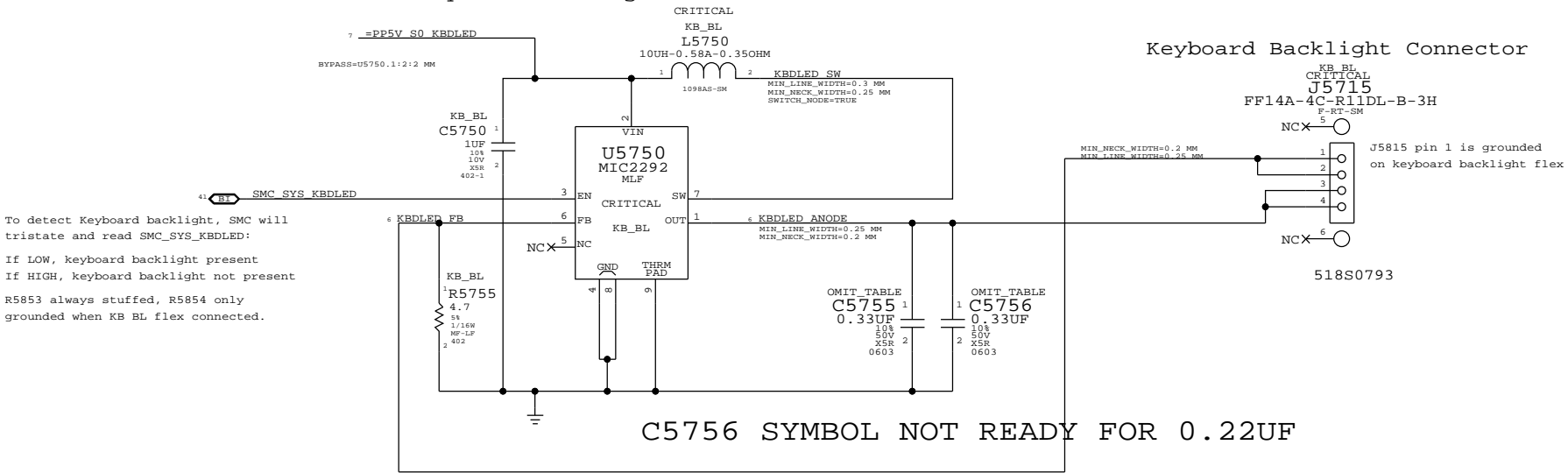
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
IPD Flex Connector



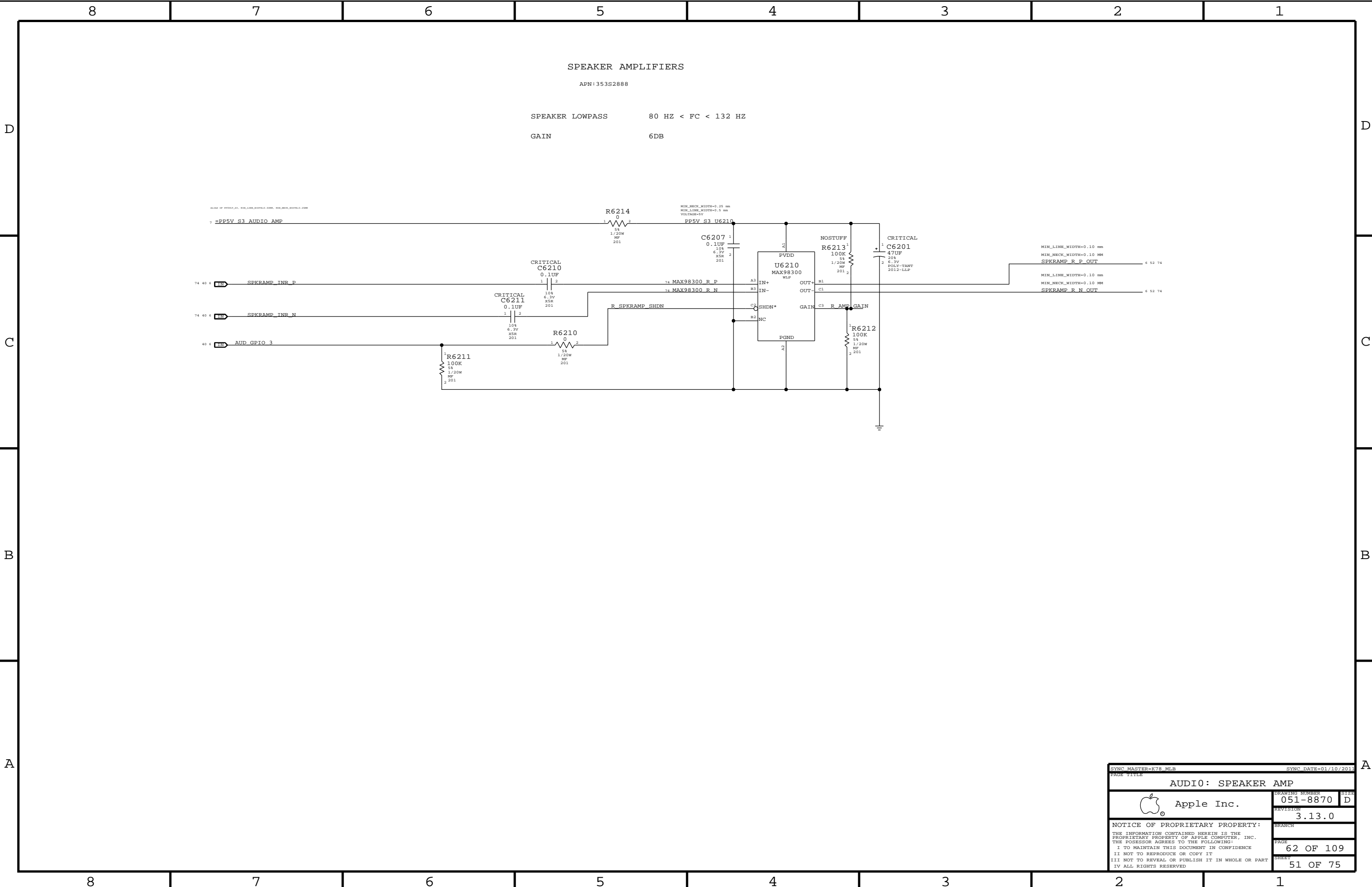
Keyboard Backlight Driver & Detection




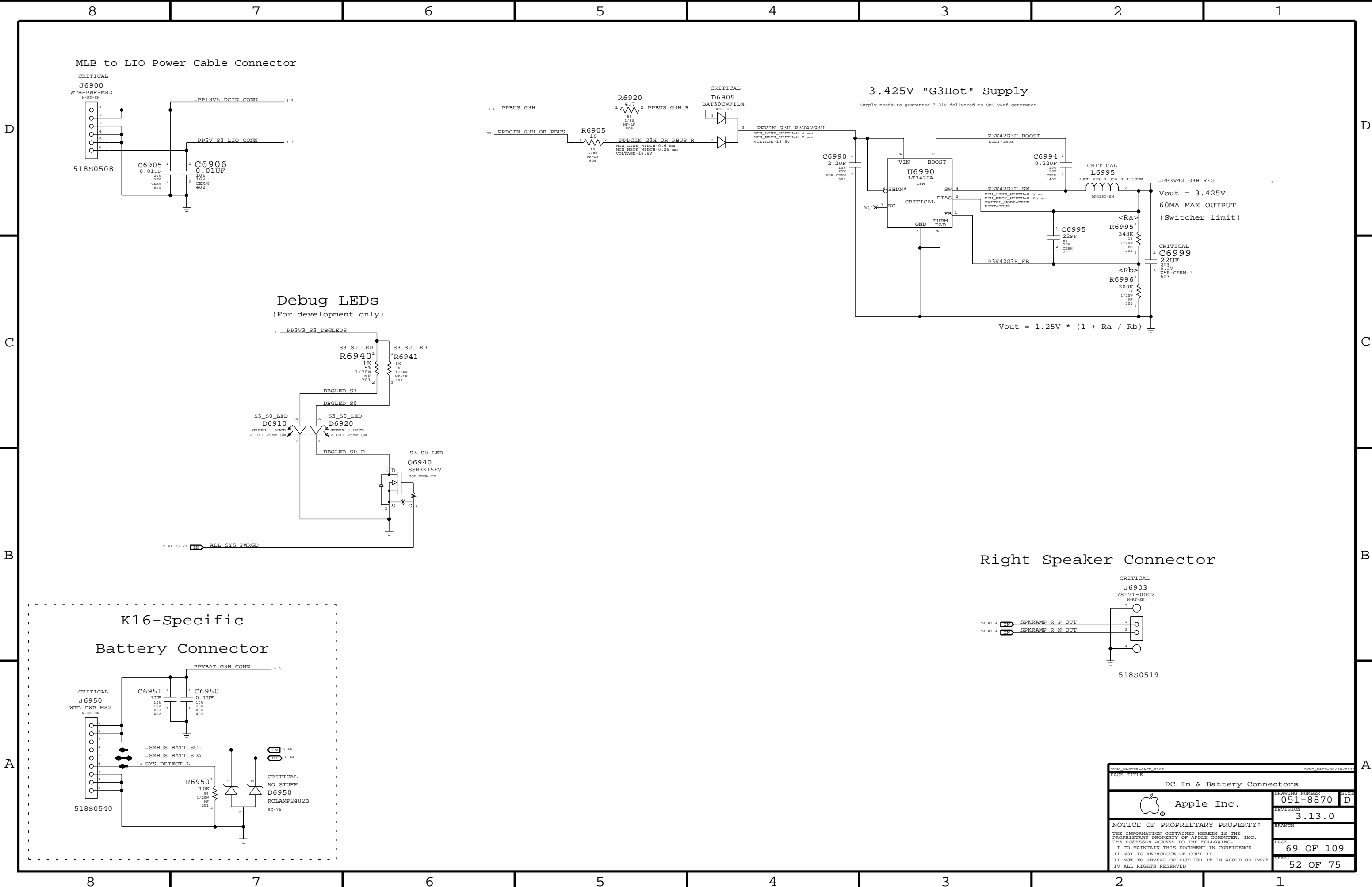
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0704	2	CAP, CER, 0.22UF, 10V, 50V, XSR, 0603	C5755, C5756		KB_BL


SYNC MASTER=K75 MLB		SYNC DATE=01/10/2013	
PAGE TITLE			
IPD / KBD Backlight			
	Apple Inc.	DRAWING NUMBER	051-8870
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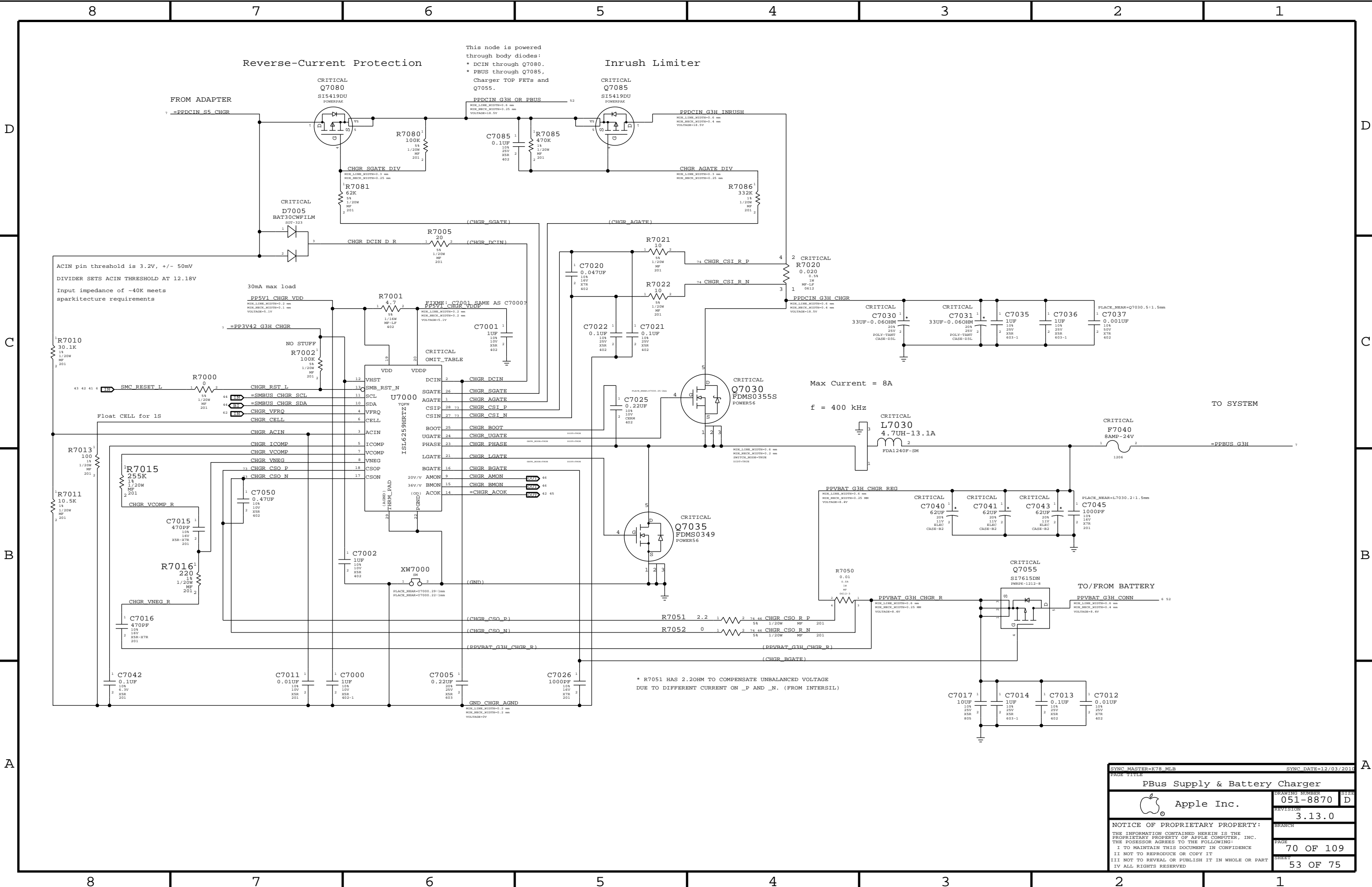




SYNC MASTER=K7S MLB		SYNC DATE=01/10/2013	
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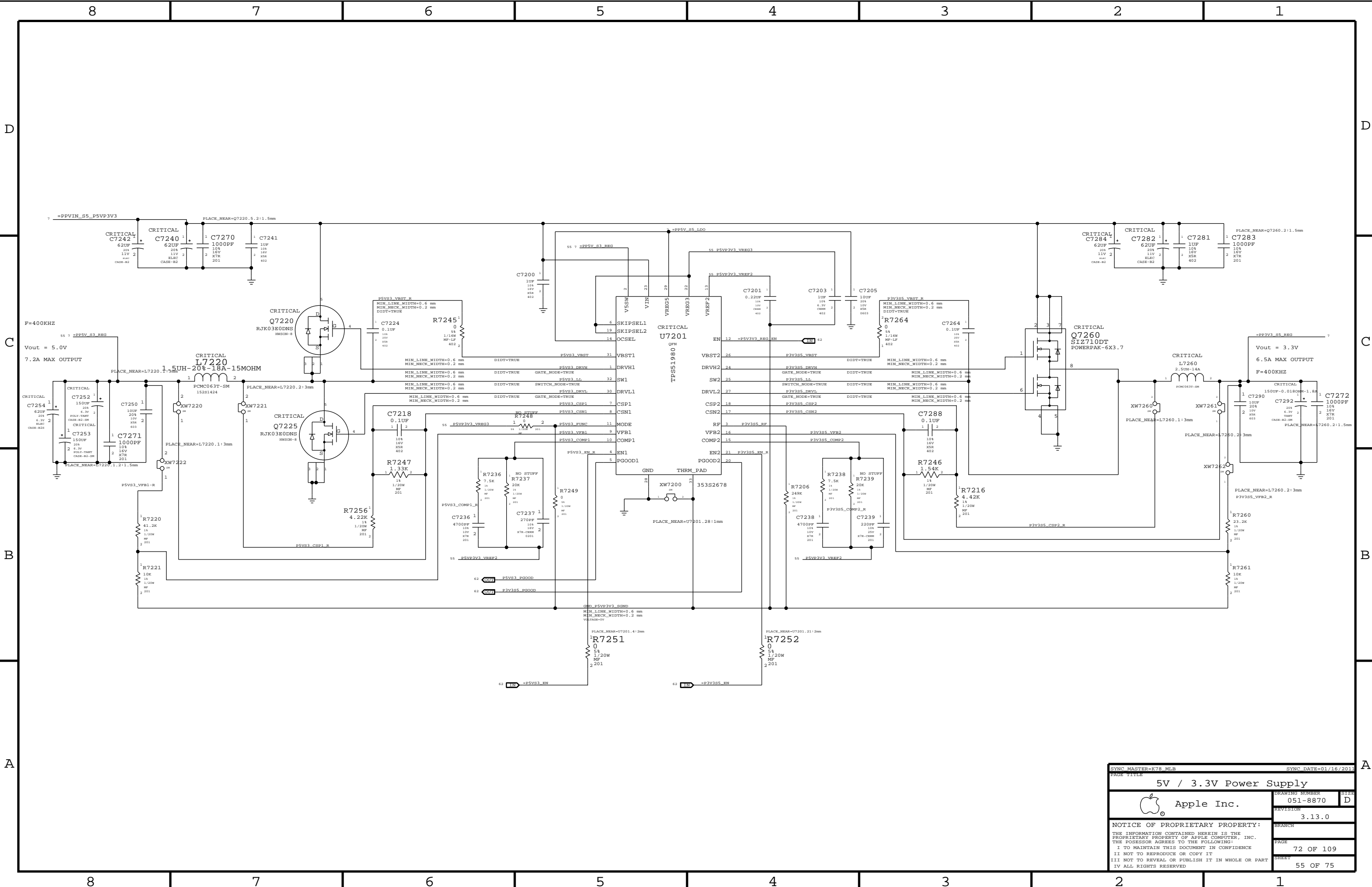



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DC-In & Battery Connectors			
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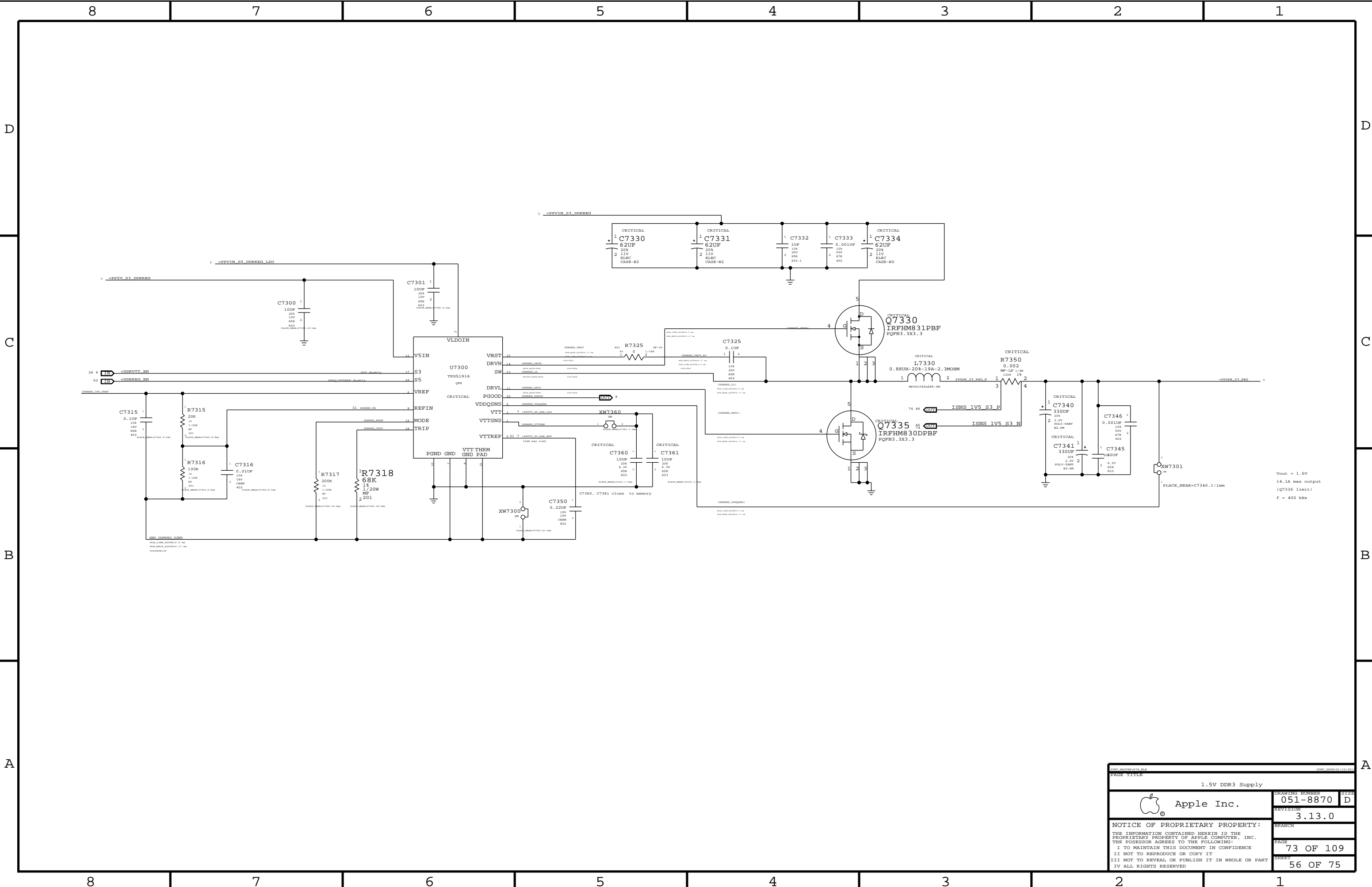






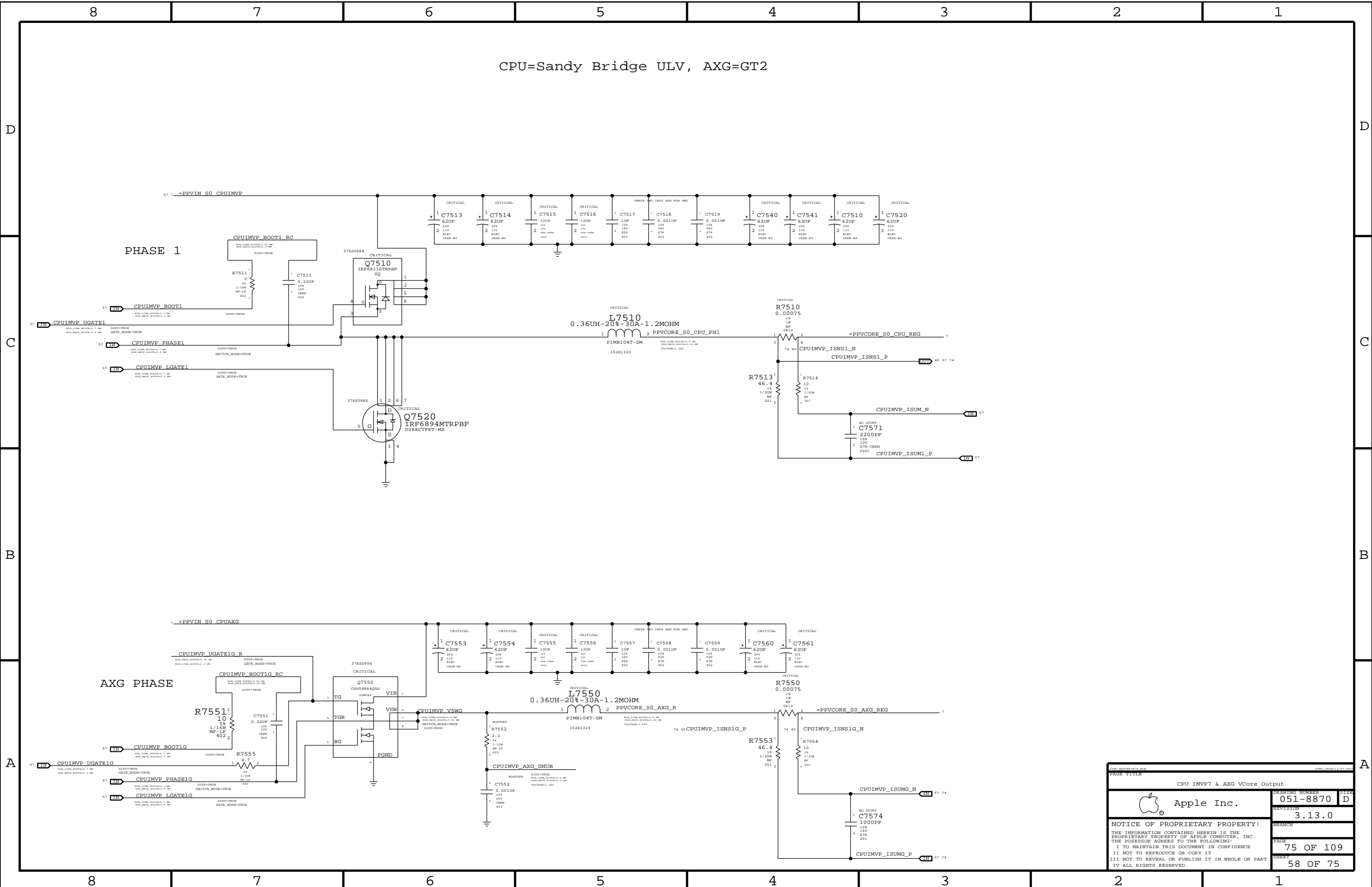


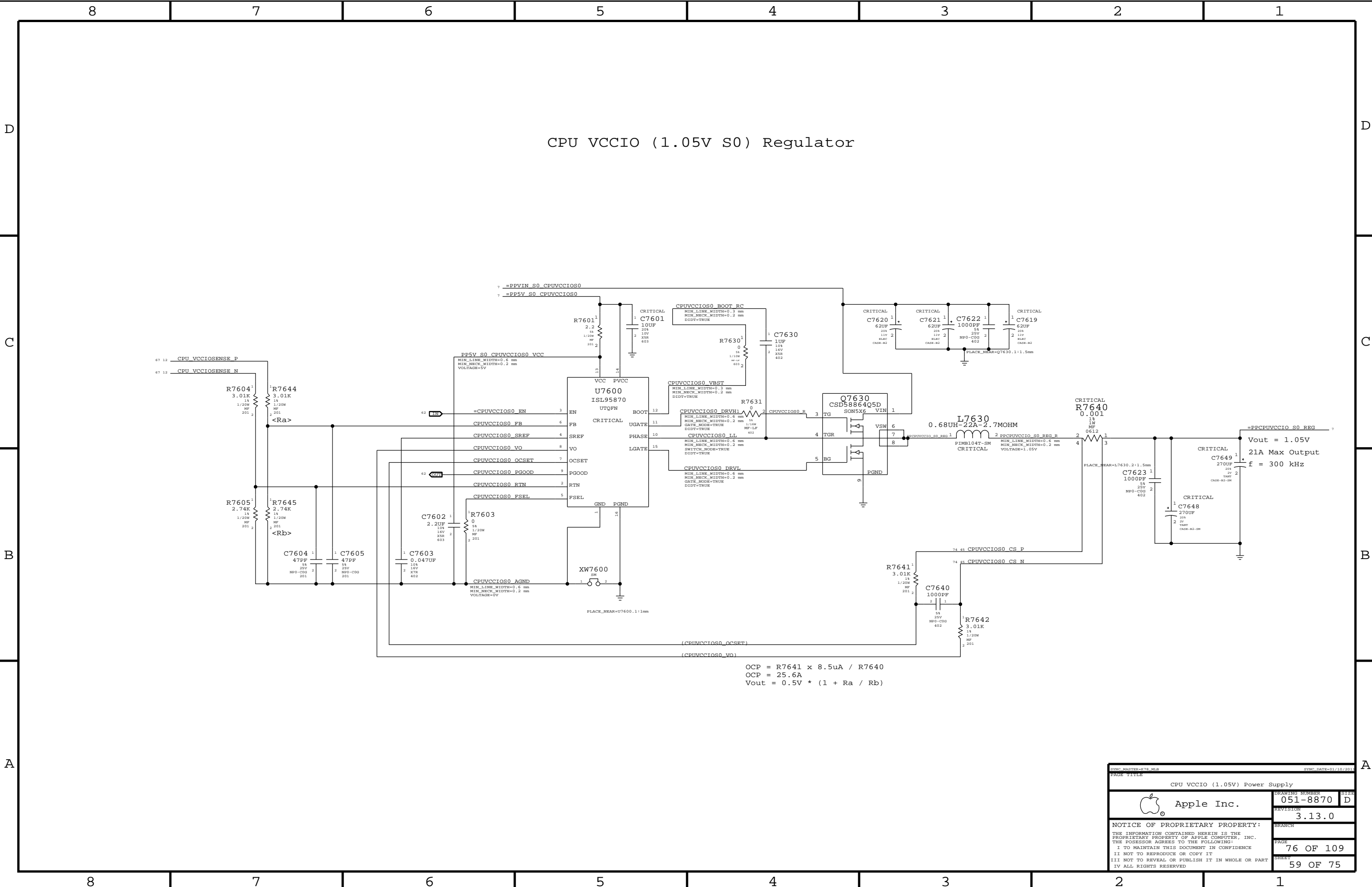
SYNC MASTER=K78 MLB		SYNC DATE=01/16/2013	
PAGE TITLE			
5V / 3.3V Power Supply			
 Apple Inc.	DRAWING NUMBER	051-8870	SIZE D
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1.5V DDR3 Supply			
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SYNCHARTER-8710-MSB		SYNCHARTER-8710-MSB	
PAGE TITLE		PAGE TITLE	
CPU VCCIO (1.05V) Power Supply		CPU VCCIO (1.05V) Power Supply	
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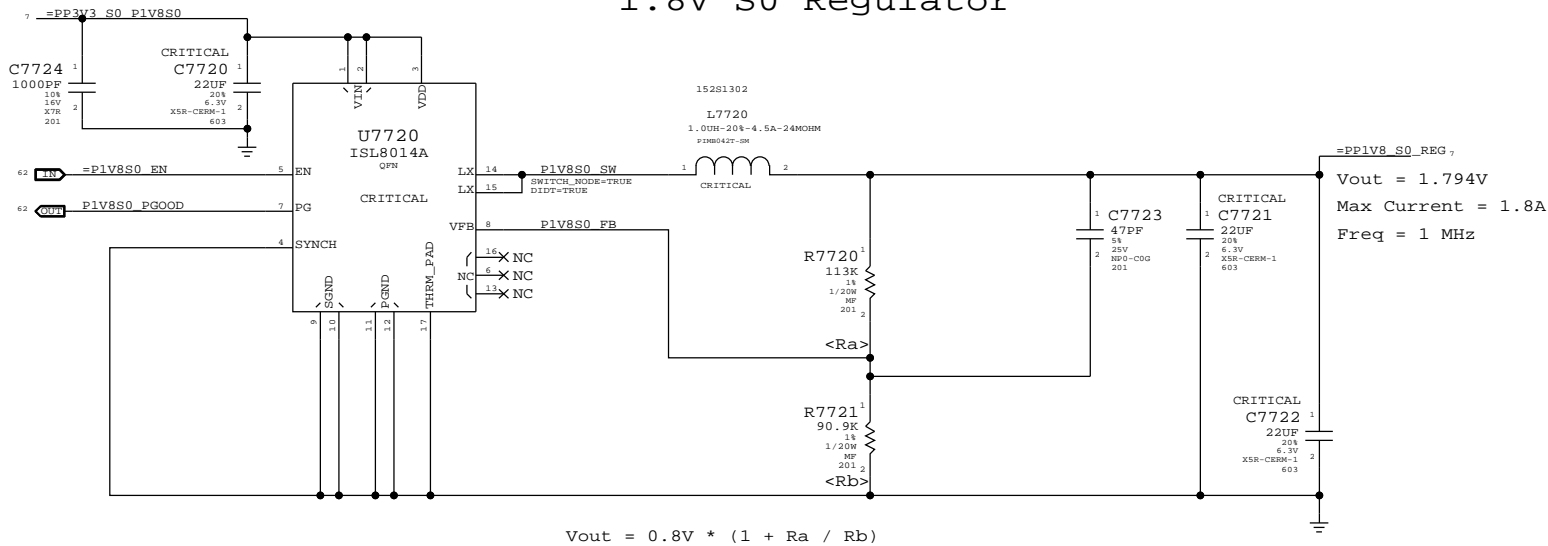
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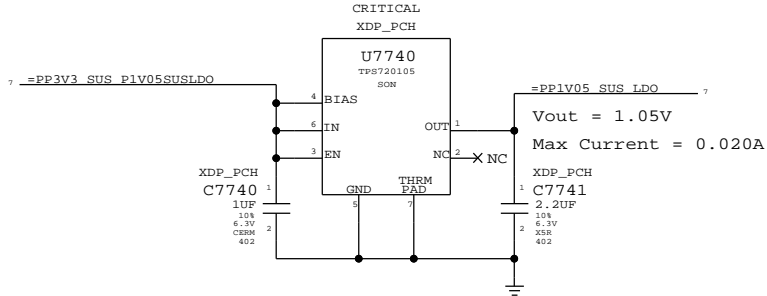
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1.8V S0 Regulator

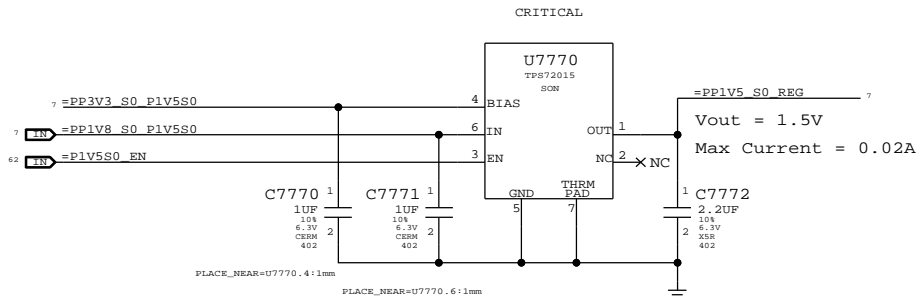


1.05V SUS LDO

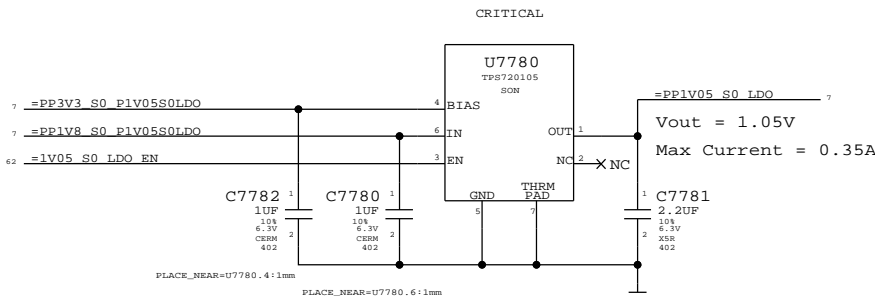
Cougar Point requires JTAG pull-ups to be powered at 1.05V when SUS suspend well is active. Pull-ups (3) must be 51 ohms to support XDP (not required in production). 70mA is required to support pull-ups. Alternative is strong voltage dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.




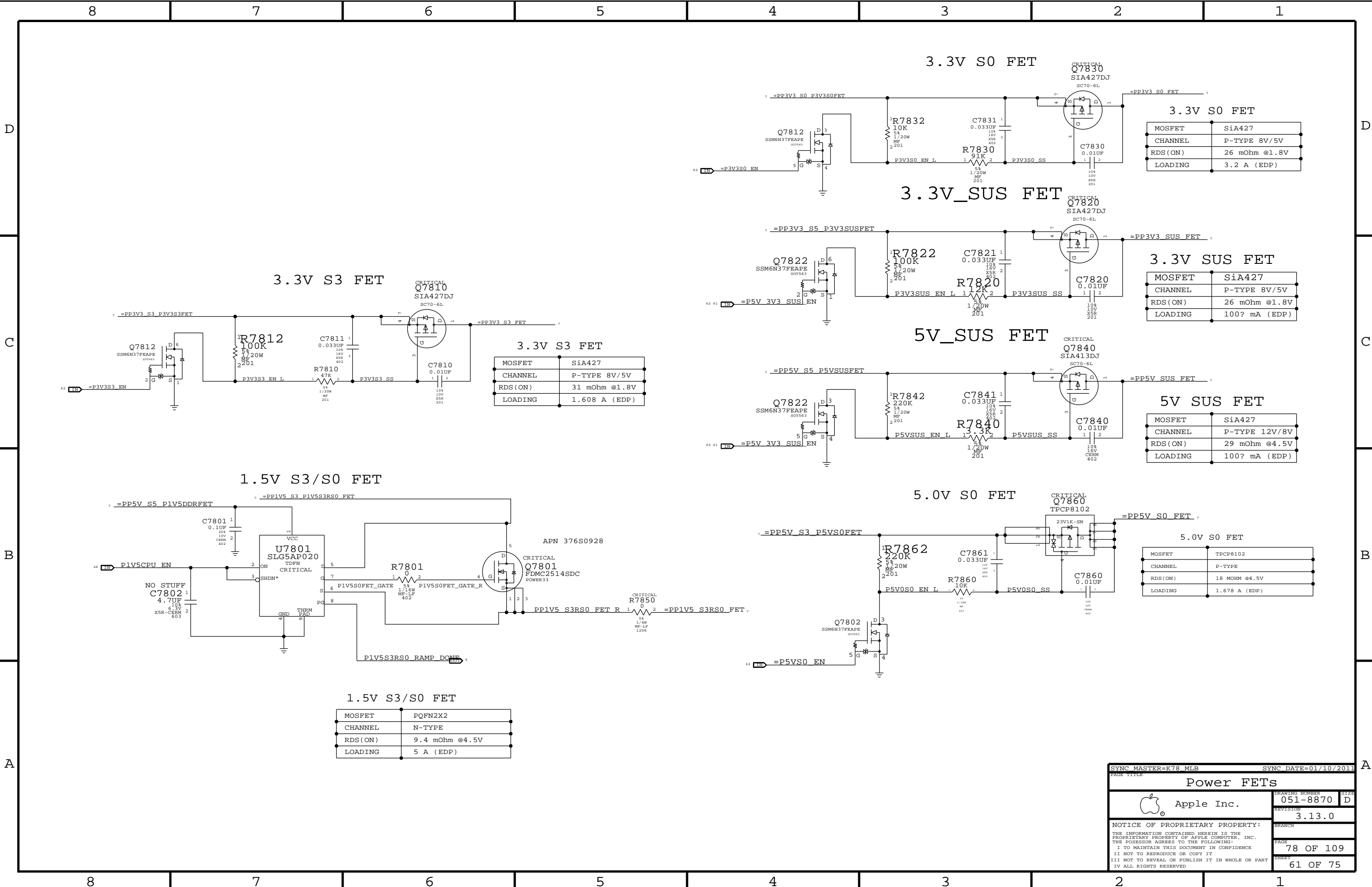
1.5V S0 LDO



1.05V S0 LDO




SYNC MASTER=K7S MLB		SYNC DATE=01/16/2013	
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Misc Power Supplies		DRAWING NUMBER	
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SYNC DATE=01/10/2011

Power FETs

 Apple Inc.

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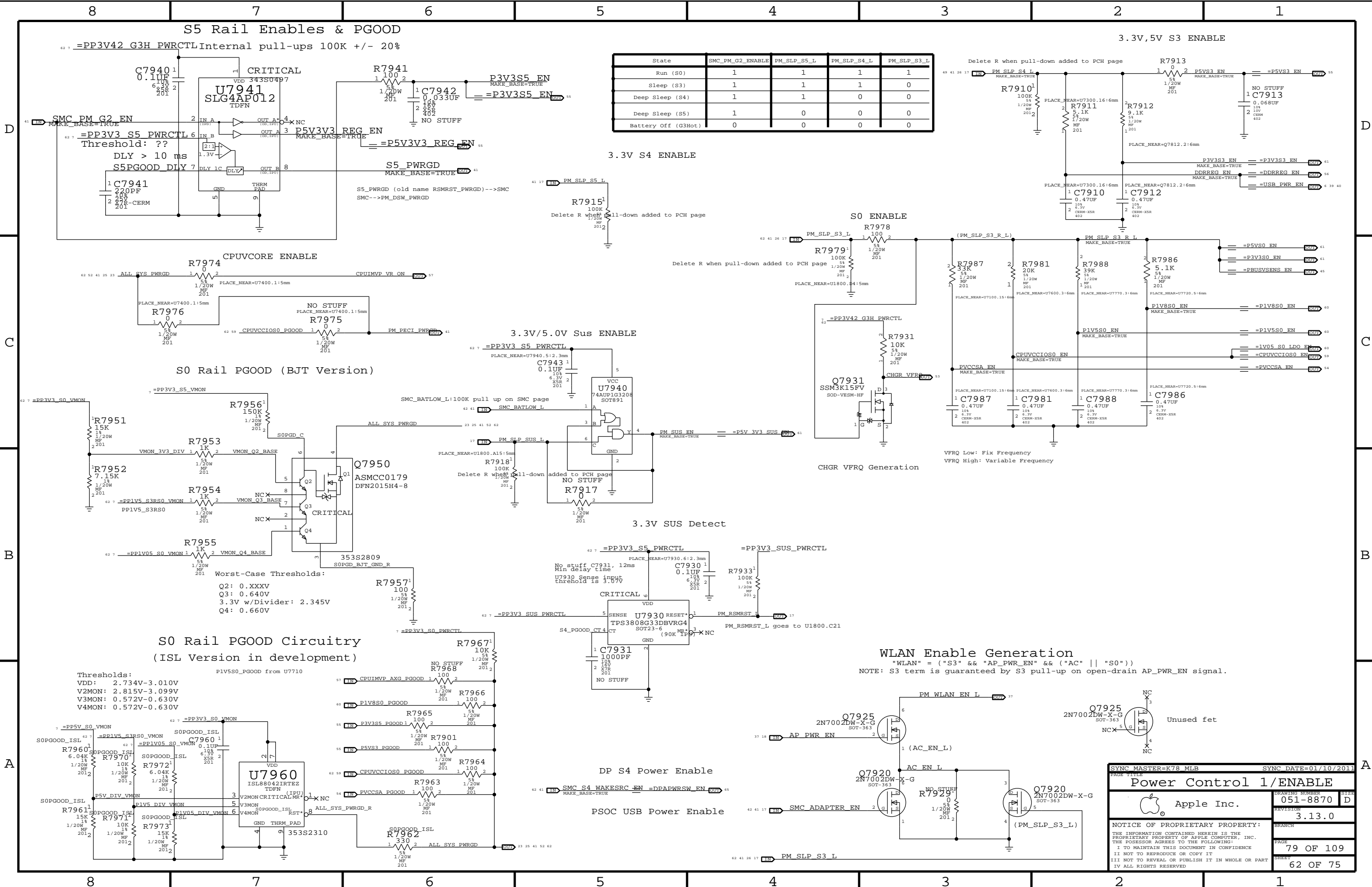
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State	SMC_PM_G2_ENABLE	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1	1
Sleep (S3)	1	1	1	0
Deep Sleep (S4)	1	1	0	0
Deep Sleep (S5)	1	0	0	0
Battery Off (G3Hot)	0	0	0	0

SYNC MASTER=K78 MLB

SYNC DATE=01/10/2011

Power Control 1/ENABLE

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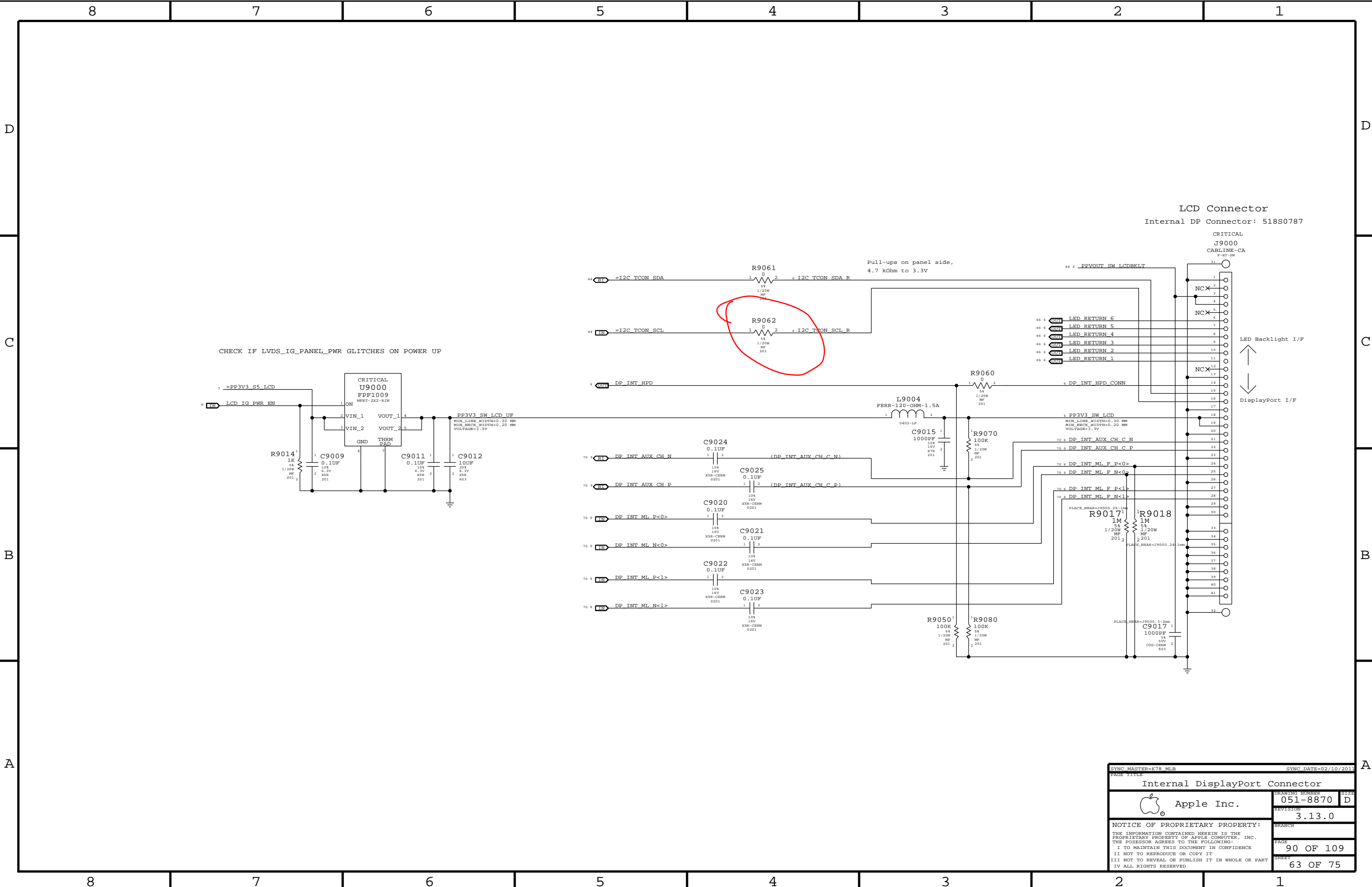
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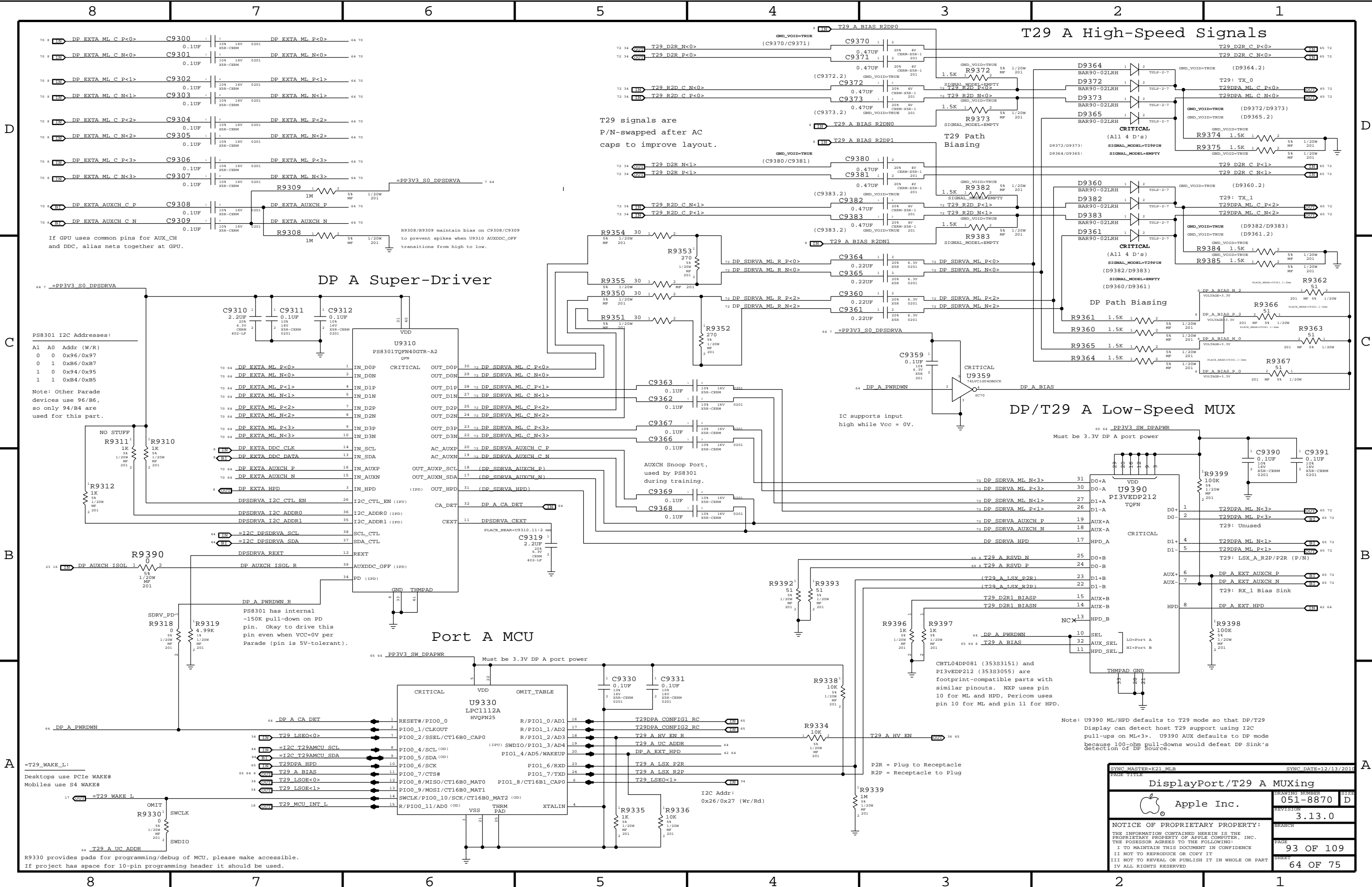
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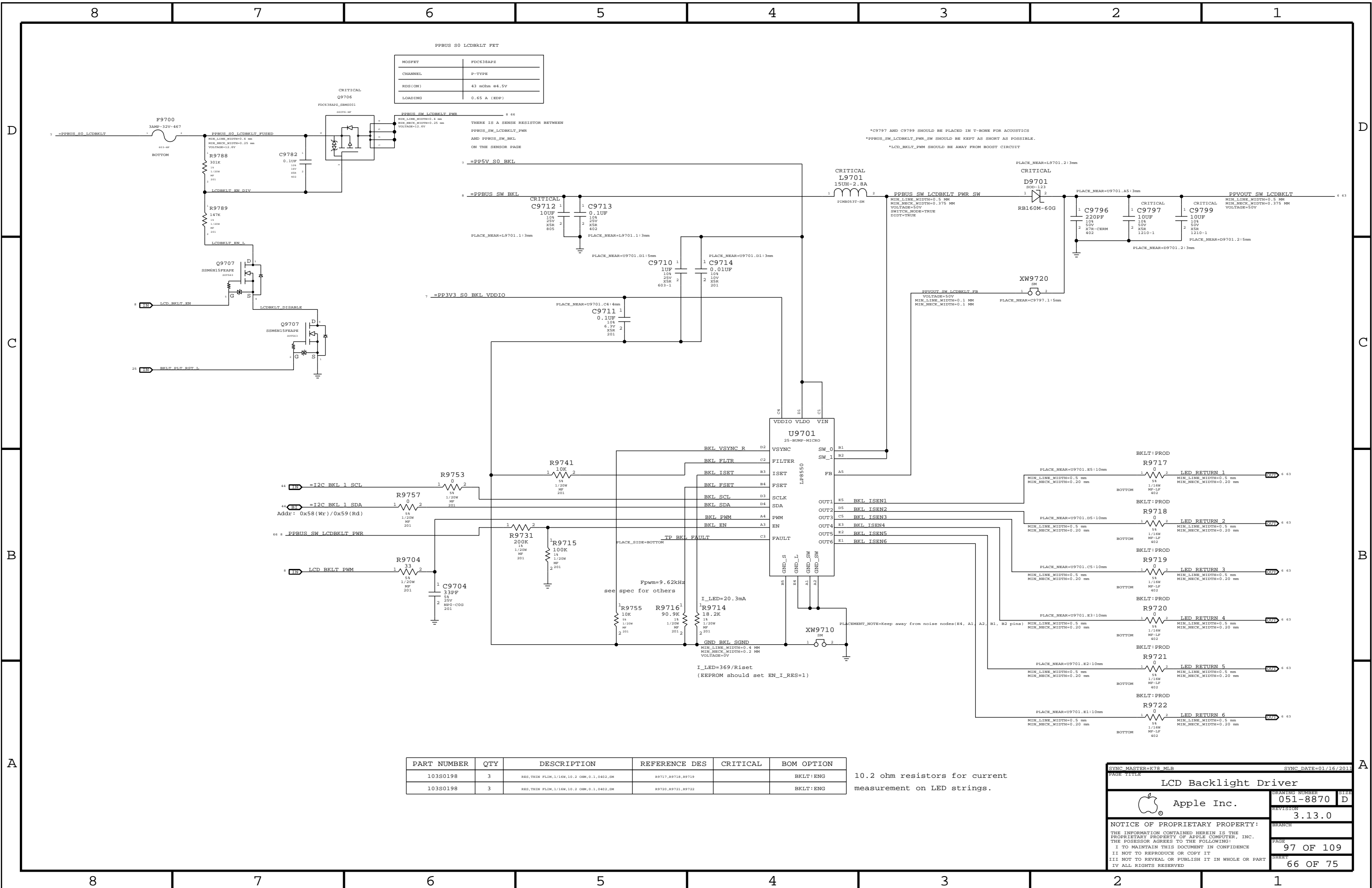
SYNC MASTER=K78 MLB		SYNC DATE=02/10/2013	
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Internal DisplayPort Connector			
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






PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3	RES,THIN FILM,1/16W,10.2 OHM,0.1,0402,0H	R9717,R9718,R9719		BKLT:ENG
103S0198	3	RES,THIN FILM,1/16W,10.2 OHM,0.1,0402,0H	R9720,R9721,R9722		BKLT:ENG

10.2 ohm resistors for current measurement on LED strings.

SYNC MASTER=K7S MLB		SYNC DATE=01/16/2013	
PAGE TITLE			
LCD Backlight Driver			
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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_37S	*	~37_OHM_SE	+37_OHM_SE	+37_OHM_SE	+37_OHM_SE	~STANDARD	~STANDARD
MEM_40S	*	~40_OHM_SE	+40_OHM_SE	+40_OHM_SE	+40_OHM_SE	~STANDARD	~STANDARD
MEM_55S	*	+55_OHM_SE	+55_OHM_SE	+55_OHM_SE	+55_OHM_SE	~STANDARD	~STANDARD
MEM_72D	*	+72_OHM_DIFF	+72_OHM_DIFF	+72_OHM_DIFF	+72_OHM_DIFF	+72_OHM_DIFF	+72_OHM_DIFF
MEM_50S	TOP_BOTTOM	Y	+50_OHM_SE	+50_OHM_SE	+50_OHM_SE	~STANDARD	~STANDARD
MEM_85D	TOP_BOTTOM	Y	+85_OHM_DIFF	+85_OHM_DIFF	+85_OHM_DIFF	+85_OHM_DIFF	+85_OHM_DIFF
MEM_50S	ISL3, ISL4, ISL9, ISL10	Y	+50_OHM_SE	+50_OHM_SE	+50_OHM_SE	~STANDARD	~STANDARD
MEM_85D	ISL3, ISL4, ISL9, ISL10	Y	+85_OHM_DIFF	+85_OHM_DIFF	+85_OHM_DIFF	+85_OHM_DIFF	+85_OHM_DIFF

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_PWR	*	MEM_2PWR
MEM_CTRL	MEM_PWR	*	MEM_2PWR
MEM_CMD	MEM_PWR	*	MEM_2PWR
MEM_DATA	MEM_PWR	*	MEM_2PWR
MEM_DQS	MEM_PWR	*	MEM_2PWR

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	MEM_2GND
MEM_CTRL	GND	*	MEM_2GND
MEM_CMD	GND	*	MEM_2GND
MEM_DATA	GND	*	MEM_2GND
MEM_DQS	GND	*	MEM_2GND

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2CLK	*	0.6 MM	?
MEM_CTRL2CTRL	*	0.2 MM	?
MEM_CMD2CTRL	*	0.2 MM	?
MEM_CMD2CMD	*	0.2 MM	?
MEM_DATA2DATA	*	0.14 MM	?
MEM_DQS2DQS	*	0.4 MM	?
MEM_MEM2OTHERMEM	*	0.4 MM	?
MEM_2PWR	*	+DWR_P2MM	?
MEM_2GND	*	+GND_P2MM	?
MEM_2OTHER	*	0.6 MM	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK
MEM_CLK	MEM_CTRL	*	MEM_MEM2OTHERMEM
MEM_CLK	MEM_CMD	*	MEM_MEM2OTHERMEM
MEM_CLK	MEM_DATA	*	MEM_MEM2OTHERMEM
MEM_CLK	MEM_DQS	*	MEM_MEM2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_MEM2OTHERMEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2CTRL
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_MEM2OTHERMEM
MEM_CMD	MEM_DQS	*	MEM_MEM2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_MEM2OTHERMEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CMD2CTRL
MEM_CTRL	MEM_DATA	*	MEM_MEM2OTHERMEM
MEM_CTRL	MEM_DQS	*	MEM_MEM2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_MEM2OTHERMEM
MEM_DQS	MEM_CTRL	*	MEM_MEM2OTHERMEM
MEM_DQS	MEM_CMD	*	MEM_MEM2OTHERMEM
MEM_DQS	MEM_DATA	*	MEM_MEM2OTHERMEM
MEM_DQS	MEM_DQS	*	MEM_DQS2DQS

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
MEM_A_CLK	MEM_72D	MEM_CLK	MEM A CLK P<5..0>	8 11 27 28 32
MEM_A_CLK	MEM_72D	MEM_CLK	MEM A CLK N<5..0>	8 11 27 28 32
MEM_A_CTRL	MEM_55S	MEM_CTRL	MEM A CKE<3..0>	8 11 27 28 32
MEM_A_CTRL	MEM_55S	MEM_CTRL	MEM A CS L<3..0>	8 11 27 28 32
MEM_A_CTRL	MEM_55S	MEM_CTRL	MEM A ODT<3..0>	8 11 27 28 32
MEM_A_CMD	MEM_55S	MEM_CMD	MEM A A<15..0>	8 11 27 28 32
MEM_A_CMD	MEM_55S	MEM_CMD	MEM A BA<2..0>	11 27 28 32
MEM_A_CMD	MEM_55S	MEM_CMD	MEM A RAS L	11 27 28 32
MEM_A_CMD	MEM_55S	MEM_CMD	MEM A CAS L	11 27 28 32
MEM_A_CMD	MEM_55S	MEM_CMD	MEM A WE L	11 27 28 32
MEM_A_DQ_BYTE0	MEM_50S	MEM_DATA	MEM A DQ<7..0>	11 27
MEM_A_DQ_BYTE1	MEM_50S	MEM_DATA	MEM A DQ<15..8>	11 27
MEM_A_DQ_BYTE2	MEM_50S	MEM_DATA	MEM A DQ<23..16>	11 27
MEM_A_DQ_BYTE3	MEM_50S	MEM_DATA	MEM A DQ<31..24>	11 27
MEM_A_DQ_BYTE4	MEM_50S	MEM_DATA	MEM A DQ<39..32>	11 28
MEM_A_DQ_BYTE5	MEM_50S	MEM_DATA	MEM A DQ<47..40>	11 28
MEM_A_DQ_BYTE6	MEM_50S	MEM_DATA	MEM A DQ<55..48>	11 28
MEM_A_DQ_BYTE7	MEM_50S	MEM_DATA	MEM A DQ<63..56>	11 28
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM A DQS P<0>	11 27
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM A DQS N<0>	11 27
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM A DQS P<1>	11 27
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM A DQS N<1>	11 27
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM A DQS P<2>	11 27
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM A DQS N<2>	11 27
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM A DQS P<3>	11 27
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM A DQS N<3>	11 27
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM A DQS P<4>	11 28
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM A DQS N<4>	11 28
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM A DQS P<5>	11 28
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM A DQS N<5>	11 28
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM A DQS P<6>	11 28
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM A DQS N<6>	11 28
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM A DQS P<7>	11 28
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM A DQS N<7>	11 28
MEM_B_CLK	MEM_72D	MEM_CLK	MEM B CLK P<5..0>	8 11 29 30 32
MEM_B_CLK	MEM_72D	MEM_CLK	MEM B CLK N<5..0>	8 11 29 30 32
MEM_B_CTRL	MEM_55S	MEM_CTRL	MEM B CKE<3..0>	8 11 29 30 32
MEM_B_CTRL	MEM_55S	MEM_CTRL	MEM B CS L<3..0>	8 11 29 30 32
MEM_B_CTRL	MEM_55S	MEM_CTRL	MEM B ODT<3..0>	8 11 29 30 32
MEM_B_CMD	MEM_55S	MEM_CMD	MEM B A<15..0>	8 11 29 30 32
MEM_B_CMD	MEM_55S	MEM_CMD	MEM B BA<2..0>	11 29 30 32
MEM_B_CMD	MEM_55S	MEM_CMD	MEM B RAS L	11 29 30 32
MEM_B_CMD	MEM_55S	MEM_CMD	MEM B CAS L	11 29 30 32
MEM_B_CMD	MEM_55S	MEM_CMD	MEM B WE L	11 29 30 32
MEM_B_DQ_BYTE0	MEM_50S	MEM_DATA	MEM B DQ<7..0>	11 29
MEM_B_DQ_BYTE1	MEM_50S	MEM_DATA	MEM B DQ<15..8>	11 29
MEM_B_DQ_BYTE2	MEM_50S	MEM_DATA	MEM B DQ<23..16>	11 29
MEM_B_DQ_BYTE3	MEM_50S	MEM_DATA	MEM B DQ<31..24>	11 29
MEM_B_DQ_BYTE4	MEM_50S	MEM_DATA	MEM B DQ<39..32>	11 30
MEM_B_DQ_BYTE5	MEM_50S	MEM_DATA	MEM B DQ<47..40>	11 30
MEM_B_DQ_BYTE6	MEM_50S	MEM_DATA	MEM B DQ<55..48>	11 30
MEM_B_DQ_BYTE7	MEM_50S	MEM_DATA	MEM B DQ<63..56>	11 30
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM B DQS P<0>	11 29
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM B DQS N<0>	11 29
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM B DQS P<1>	11 29
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM B DQS N<1>	11 29
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM B DQS P<2>	11 29
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM B DQS N<2>	11 29
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM B DQS P<3>	11 29
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM B DQS N<3>	11 29
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM B DQS P<4>	11 30
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM B DQS N<4>	11 30
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM B DQS P<5>	11 30
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM B DQS N<5>	11 30
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM B DQS P<6>	11 30
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM B DQS N<6>	11 30
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM B DQS P<7>	11 30
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM B DQS N<7>	11 30
		MEM_PWR	PP1V5 S3RS0	7
		MEM_PWR	PP1V5 S3	7
		MEM_PWR	PP0V75 S3 MEM VREFCA A	27 28 29 30 31
		MEM_PWR	PP0V75 S3 MEM VREFDQ A	9 27 28 29 30 31

Need to support MEM\_\*-style wildcards!

DDR3: Sandybridge SFF 2C when routed on Type-3 (Through hole) should follow +PGA guidelines per Huron River SFF DG rev1.0 (#438297). DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement. DQ to DQS matching per byte lane should be within 0.127mm. DQS to clock matching should be within [CLK-63.5mm] and [CLK+38.1mm]. CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.0508mm. CONTROL signals should be matched within [CLK-2.54mm] to [CLK+0.0mm] of CLK pairs. A/BA/CMD signals should be matched within [CLK-12.7mm] to [CLK+12.7mm] of CLK pairs A/BA/CMD signals to each other should match within 5.08mm. DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric. Maximum length of any signal from die pad to SODIMM pad is 119.83mm, from processor ball to SODIMM pad is 88.9mm. SOURCE: Huron River Platform DG, Rev 1.01 (#436735), Section 2.5

Memory Constraints

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## Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
LVDS_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.  
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.  
DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.  
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.  
SOURCE: MCP79 interface DG (DG-03328-001\_v0D), Sections 2.5.3 & 2.5.4.

## SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	-90_OHM_DIFF	-90_OHM_DIFF	-90_OHM_DIFF	-90_OHM_DIFF	-90_OHM_DIFF	-90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4x_DIELECTRIC	?
SATA_1COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.7.1.

## USB 2.0 Interface Constraints


PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_BIAS	*	-STANDARD	8 MIL	8 MIL	-STANDARD	-STANDARD	-STANDARD
USB_8SD	*	-85_OHM_DIFF	-85_OHM_DIFF	-85_OHM_DIFF	-85_OHM_DIFF	-85_OHM_DIFF	-85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	~2x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ixex Peak M (DG-398905-398905\_v1.5), Section 3.8

## PCH Net Properties

ELECTRICAL_CONSTRAINT_SET		SET_TYPE		
		PHYSICAL	SPACING	
DP_ML	DP_85D	DISPLAYPORT	DP IG ML P<3..0>	8
DP_ML	DP_85D	DISPLAYPORT	DP IG ML N<3..0>	8
DP_EXT_AUXCH	DP_85D	DISPLAYPORT	DP IG AUX CH P	8
DP_EXT_AUXCH	DP_85D	DISPLAYPORT	DP IG AUX CH N	8
LVDS_IG_A_CLK	LVDS_90D	LVDS	LVDS IG A CLK P	
LVDS_IG_A_CLK	LVDS_90D	LVDS	LVDS IG A CLK N	
LVDS_IG_A_DATA	LVDS_90D	LVDS	LVDS IG A DATA P<2..0>	
LVDS_IG_A_DATA	LVDS_90D	LVDS	LVDS IG A DATA N<2..0>	
	LVDS_90D	LVDS	LVDS IG A DATA P<3>	8
	LVDS_90D	LVDS	LVDS IG A DATA N<3>	8
	LVDS_90D	LVDS	LVDS IG B DATA P<3..0>	8
	LVDS_90D	LVDS	LVDS IG B DATA N<3..0>	8
	LVDS_90D	LVDS	LVDS IG B CLK P	
	LVDS_90D	LVDS	LVDS IG B CLK N	8
	SATA_90D	SATA	SATA HDD R2D C P	16 38
	SATA_90D	SATA	SATA HDD R2D C N	16 38
SATA_HDD_R2D	SATA_90D	SATA	SATA HDD R2D P	6 38
SATA_HDD_R2D	SATA_90D	SATA	SATA HDD R2D N	6 38
SATA_HDD_D2R	SATA_90D	SATA	SATA HDD D2R P	16 38
SATA_HDD_D2R	SATA_90D	SATA	SATA HDD D2R N	16 38
	SATA_90D	SATA	SATA HDD D2R C P	6 38
	SATA_90D	SATA	SATA HDD D2R C N	6 38
	SATA_90D	SATA	SATA ODD R2D C P	8 16
	SATA_90D	SATA	SATA ODD R2D C N	8 16
SATA_ODD_R2D	SATA_90D	SATA	SATA ODD R2D P	
SATA_ODD_R2D	SATA_90D	SATA	SATA ODD R2D N	
SATA_ODD_D2R	SATA_90D	SATA	SATA ODD D2R P	8 16
SATA_ODD_D2R	SATA_90D	SATA	SATA ODD D2R N	8 16
	SATA_90D	SATA	SATA HDD R2D RC P	
	SATA_90D	SATA	SATA HDD R2D RC N	
	SATA_90D	SATA	SATA HDD D2R RC P	
	SATA_90D	SATA	SATA HDD D2R RC N	
PCH_SATA_ICOMP		SATA_ICOMP	PCH SATAICOMP	16
USB_HUB1_UP	USB_85D	USB	USB HUB1 UP P	18 24
	USB_85D	USB	USB HUB1 UP N	18 24
USB_HUB2_UP	USB_85D	USB	USB HUB2 UP P	18 24
	USB_85D	USB	USB HUB2 UP N	18 24
USB_EXT_A	USB_85D	USB	USB EXT_A P	24 39
USB_EXT_A	USB_85D	USB	USB EXT_A N	24 39
USB_EXTB	USB_85D	USB	USB EXT_B P	
	USB_85D	USB	USB EXT_B N	
USB_EXT_C	USB_85D	USB	USB EXT_C P	
	USB_85D	USB	USB EXT_C N	
USB_EXTD	USB_85D	USB	USB EXT_D P	6 24
	USB_85D	USB	USB EXT_D N	6 24
USB_EXTD	USB_85D	USB	USB T29A P	8 24
	USB_85D	USB	USB T29A N	8 24
	USB_85D	USB	T29 A RSVD P	8 64
	USB_85D	USB	T29 A RSVD N	8 64
USB_CAMERA	USB_85D	USB	USB CAMERA P	6 18
	USB_85D	USB	USB CAMERA N	6 18
USB_CAMERA	USB_85D	USB	USB CAMERA CONN P	
	USB_85D	USB	USB CAMERA CONN N	
USB_BT	USB_85D	USB	USB BT P	6 24
USB_BT	USB_85D	USB	USB BT N	6 24
USB_TPAD	USB_85D	USB	USB TPAD P	49
	USB_85D	USB	USB TPAD N	49
USB_IR	USB_85D	USB	USB IR P	
	USB_85D	USB	USB IR N	
USB_SDCARD	USB_85D	USB	USB SDCARD P	24 33
	USB_85D	USB	USB SDCARD N	24 33
USB_BRCRYPT	USB_85D	USB	USB BRCRYPT P	
	USB_85D	USB	USB BRCRYPT N	
PCH_USB_RBIAS	PCH_USB_RBIAS		PCH USB RBIAS	18
PCH_DIFCLK_UNUSED	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M PCH P	16 25
PCH_DIFCLK_UNUSED	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M PCH N	16 25
	CLK_PCIE_90D	CLK_PCIE	FSB CLK133M PCH P	8
	CLK_PCIE_90D	CLK_PCIE	FSB CLK133M PCH N	8
PCH_DIFCLK_UNUSED	CLK_PCIE_90D	CLK_PCIE	PCH CLK96M DOT P	16 25
PCH_DIFCLK_UNUSED	CLK_PCIE_90D	CLK_PCIE	PCH CLK96M DOT N	16 25
PCH_DIFCLK_UNUSED	CLK_PCIE_90D	CLK_PCIE	PCH CLK100M SATA P	16 25
PCH_DIFCLK_UNUSED	CLK_PCIE_90D	CLK_PCIE	PCH CLK100M SATA N	16 25
	CPU_50S	CLK_PCIE	PCH CLK14P3M REFCLK	16 25
	CPU_50S	CLK_PCIE	PCH CLK33M PCIIIN	16 25

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8	7	6	5	4	3	2	1		
LPC Bus Constraints									
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
LPC_50S		*	+50_OHM_SE	+50_OHM_SE	+50_OHM_SE	+50_OHM_SE	+STANDARD	+STANDARD	
CLK_LPC_50S		*	+50_OHM_SE	+50_OHM_SE	+50_OHM_SE	+50_OHM_SE	+STANDARD	+STANDARD	
SPACING_RULE_SET		LAYER	LINE-TO-LINE SPACING	WEIGHT					
LPC		*	6 MIL	?					
CLK_LPC		*	8 MIL	?					
SOURCE: Calpella Platform Design Guide for Ibox Peak M (DG-398905-398905_v1.5), Section 3.15									
SMBus Interface Constraints									
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
SMB_50S		*	+50_OHM_SE	+50_OHM_SE	+50_OHM_SE	+50_OHM_SE	+STANDARD	+STANDARD	
SPACING_RULE_SET		LAYER	LINE-TO-LINE SPACING	WEIGHT					
SMB		*	+2x_DIELECTRIC	?					
HD Audio Interface Constraints									
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
HDA_50S		*	+50_OHM_SE	+50_OHM_SE	+50_OHM_SE	+50_OHM_SE	+STANDARD	+STANDARD	
SPACING_RULE_SET		LAYER	LINE-TO-LINE SPACING	WEIGHT					
HDA		*	+2x_DIELECTRIC	?					
SOURCE: Calpella Platform Design Guide for Ibox Peak M (DG-398905-398905_v1.5), Section 3.15									
SIO Signal Constraints									
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
CLK_SLOW_55S		*	+55_OHM_SE	+55_OHM_SE	+55_OHM_SE	+55_OHM_SE	+STANDARD	+STANDARD	
SPACING_RULE_SET		LAYER	LINE-TO-LINE SPACING	WEIGHT					
CLK_SLOW		*	8 MIL	?					
SPI Interface Constraints									
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
SPI_55S		*	+55_OHM_SE	+55_OHM_SE	+55_OHM_SE	+55_OHM_SE	+STANDARD	+STANDARD	
SPACING_RULE_SET		LAYER	LINE-TO-LINE SPACING	WEIGHT					
SPI		*	8 MIL	?					
DisplayPort Signal Constraints									
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
DP_85D		*	+85_OHM_DIFF	+85_OHM_DIFF	+85_OHM_DIFF	+85_OHM_DIFF	+85_OHM_DIFF	+85_OHM_DIFF	
SPACING_RULE_SET		LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET		LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT		*	+3x_DIELECTRIC	?	DISPLAYPORT		TOP_BOTTOM	+4x_DIELECTRIC	?
PCI-Express Signal Constraints									
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
PCIE_85D		*	+85_OHM_DIFF	+85_OHM_DIFF	+85_OHM_DIFF	+85_OHM_DIFF	+85_OHM_DIFF	+85_OHM_DIFF	
CLK_PCIE_90D		*	+90_OHM_DIFF	+90_OHM_DIFF	+90_OHM_DIFF	+90_OHM_DIFF	+90_OHM_DIFF	+90_OHM_DIFF	
SPACING_RULE_SET		LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET		LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE		*	+3x_DIELECTRIC	?	PCIE		TOP_BOTTOM	+4x_DIELECTRIC	?
CLK_PCIE		*	20 MIL	?					
System Clock Signal Constraints									
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
CLK_SLOW_55S		*	+55_OHM_SE	+55_OHM_SE	+55_OHM_SE	+55_OHM_SE	+STANDARD	+STANDARD	
CLK_25M_55S		*	+55_OHM_SE	+55_OHM_SE	+55_OHM_SE	+55_OHM_SE	+STANDARD	+STANDARD	
SPACING_RULE_SET		LAYER	LINE-TO-LINE SPACING	WEIGHT					
CLK_SLOW		*	+2x_DIELECTRIC	?					
CLK_25M		*	+5x_DIELECTRIC	?					
NOTE: 25MHz system clocks very sensitive to noise.									
PCH Net Properties									
ELECTRICAL_CONSTRAINT_SET		NET_TYPE							
		PHYSICAL	SPACING						
LPC_AD		LPC_50S	LPC	LPC AD<3..0>					
LPC_FRAME_L		LPC_50S	LPC	LPC FRAME_L					
LPC_RESET_L		LPC_50S	LPC	LPC RESET_L					
LPC_CLK33M		CLK_LPC_50S	CLK_LPC	LPC CLK33M SMC R					
LPC_CLK33M		CLK_LPC_50S	CLK_LPC	LPC CLK33M SMC					
LPC_CLK33M		CLK_LPC_50S	CLK_LPC	LPC CLK33M LPCPLUS					
SMBUS_PCH_CLK		SMB_50S	SMB	SMBUS PCH CLK					
SMBUS_PCH_DATA		SMB_50S	SMB	SMBUS PCH DATA					
SMBUS_PCH_0_CLK		SMB_50S	SMB	SML PCH_0_CLK					
SMBUS_PCH_0_DATA		SMB_50S	SMB	SML PCH_0 DATA					
SMBUS_PCH_1_CLK		SMB_50S	SMB	SML PCH_1_CLK					
SMBUS_PCH_1_DATA		SMB_50S	SMB	SML PCH_1 DATA					
HDA_BIT_CLK		HDA_50S	HDA	HDA BIT_CLK					
HDA_50S		HDA_50S	HDA	HDA BIT_CLK_R					
HDA_SYNC		HDA_50S	HDA	HDA SYNC					
HDA_50S		HDA_50S	HDA	HDA SYNC_R					
HDA_RST_L		HDA_50S	HDA	HDA_RST_R_L					
HDA_50S		HDA_50S	HDA	HDA_RST_L					
HDA_SDIO0		HDA_50S	HDA	HDA_SDIO0					
HDA_50S		HDA_50S	HDA	AUD_SDI_R					
HDA_SDO0T		HDA_50S	HDA	HDA_SDO0T					
HDA_50S		HDA_50S	HDA	HDA_SDO0T_R					
PM_SUS_CLK		CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK					
SPI_CLK		SPI_55S	SPI	SPI_CLK_R					
SPI_55S		SPI_55S	SPI	SPI_CLK					
SPI_MOSI		SPI_55S	SPI	SPI_MOSI_R					
SPI_55S		SPI_55S	SPI	SPI_MOSI					
SPI_MISO		SPI_55S	SPI	SPI_MISO					
SPI_CS0		SPI_55S	SPI	SPI_CS0_R_L					
SPI_55S		SPI_55S	SPI	SPI_CS0_L					
SPI_55S		SPI_55S	SPI	SPI_MLB_CLK					
SPI_55S		SPI_55S	SPI	SPI_MLB_MOSI					
SPI_55S		SPI_55S	SPI	SPI_MLB_MISO					
SPI_55S		SPI_55S	SPI	SPI_MLB_CS_L					
PCIE_85D		PCIE	PCIE	PCIE ENET R2D P					
PCIE_85D		PCIE	PCIE	PCIE ENET R2D N					
PCIE_85D		PCIE	PCIE	PCIE ENET R2D C P					
PCIE_85D		PCIE	PCIE	PCIE ENET R2D C N					
PCIE_85D		PCIE	PCIE	PCIE ENET D2R P					
PCIE_85D		PCIE	PCIE	PCIE ENET D2R N					
PCIE_85D		PCIE	PCIE	PCIE ENET D2R C P					
PCIE_85D		PCIE	PCIE	PCIE ENET D2R C N					
PCIE_85D		PCIE	PCIE	PCIE AP R2D P					
PCIE_85D		PCIE	PCIE	PCIE AP R2D N					
PCIE_85D		PCIE	PCIE	PCIE AP R2D C P					
PCIE_85D		PCIE	PCIE	PCIE AP R2D C N					
PCIE_85D		PCIE	PCIE	PCIE AP D2R P					
PCIE_85D		PCIE	PCIE	PCIE AP D2R N					
PCIE_85D		PCIE	PCIE	PCIE FW R2D P					
PCIE_85D		PCIE	PCIE	PCIE FW R2D N					
PCIE_85D		PCIE	PCIE	PCIE FW R2D C P					
PCIE_85D		PCIE	PCIE	PCIE FW R2D C N					
PCIE_85D		PCIE	PCIE	PCIE FW D2R P					
PCIE_85D		PCIE	PCIE	PCIE FW D2R N					
PCIE_85D		PCIE	PCIE	PCIE FW D2R C P					
PCIE_85D		PCIE	PCIE	PCIE FW D2R C N					
PCIE_85D		PCIE	PCIE	CONN_PCIE AP D2R P					
PCIE_85D		PCIE	PCIE	CONN_PCIE AP D2R N					
PCIE_85D		PCIE	PCIE	CONN_PCIE AP R2D P					
PCIE_85D		PCIE	PCIE	CONN_PCIE AP R2D N					
CLK_PCIE_90D		CLK_PCIE_90D	CLK_PCIE	PEG CLK100M P					
CLK_PCIE_90D		CLK_PCIE_90D	CLK_PCIE	PEG CLK100M N					
CLK_PCIE_90D		CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M ENET P					
CLK_PCIE_90D		CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M ENET N					
CLK_PCIE_90D		CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M AP P					
CLK_PCIE_90D		CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M AP N					
CLK_PCIE_90D		CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M FW P					
CLK_PCIE_90D		CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M FW N					
CLK_PCIE_90D		CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M EXCARD P					
CLK_PCIE_90D		CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M EXCARD N					
CPU_27P4S		CPU_COMP	CPU	PCH VSS NCTF<1>					
CPU_27P4S		CPU_COMP	CPU	PCH VSS NCTF<2>					
CPU_27P4S		CPU_COMP	CPU	PCH VSS NCTF<5>					
CPU_27P4S		CPU_COMP	CPU	TP_PCH VSS NCTF<7>					
CPU_27P4S		CPU_COMP	CPU	PCH VSS NCTF<9>					
CPU_27P4S		CPU_COMP	CPU	PCH VSS NCTF<9>					
CPU_27P4S		CPU_COMP	CPU	PCH VSS NCTF<11>					
CPU_27P4S		CPU_COMP	CPU	PCH VSS NCTF<12>					
CPU_27P4S		CPU_COMP	CPU	PCH VSS NCTF<15>					
CPU_27P4S		CPU_COMP	CPU	PCH VSS NCTF<17>					
CPU_27P4S		CPU_COMP	CPU	PCH VSS NCTF<19>					
CPU_27P4S		CPU_COMP	CPU	PCH VSS NCTF<21>					
CPU_27P4S		CPU_COMP	CPU	PCH VSS NCTF<22>					
CPU_27P4S		CPU_COMP	CPU	PCH VSS NCTF<25>					
CPU_27P4S		CPU_COMP	CPU	PCH VSS NCTF<27>					
CPU_27P4S		CPU_COMP	CPU	PCH VSS NCTF<29>					
Chipset Net Properties									
ELECTRICAL_CONSTRAINT_SET		NET_TYPE							
		PHYSICAL	SPACING						
DP_EXTN_ML		DP_85D	DISPLAYPORT	DP_EXTN_ML C P<3..0>					
DP_EXTN_ML		DP_85D	DISPLAYPORT	DP_EXTN_ML C N<3..0>					
DP_EXTN_ML		DP_85D	DISPLAYPORT	DP_EXTN_ML P<3..0>					
DP_EXTN_ML		DP_85D	DISPLAYPORT	DP_EXTN_ML N<3..0>					
DP_EXTN_AUXCH		DP_85D	DISPLAYPORT	DP_EXTN_AUXCH C P					
DP_EXTN_AUXCH		DP_85D	DISPLAYPORT	DP_EXTN_AUXCH C N					
DP_EXTN_AUXCH		DP_85D	DISPLAYPORT	DP_EXTN_AUXCH P					
DP_EXTN_AUXCH		DP_85D	DISPLAYPORT	DP_EXTN_AUXCH N					
DP_INT_ML		DP_85D	DISPLAYPORT	DP_INT_ML C P<3..0>					
DP_INT_ML		DP_85D	DISPLAYPORT	DP_INT_ML C N<3..0>					
DP_INT_ML		DP_85D	DISPLAYPORT	DP_INT_ML N<3..0>					
DP_INT_ML		DP_85D	DISPLAYPORT	DP_INT_ML F P<3..0>					
DP_INT_AUXCH		DP_85D	DISPLAYPORT	DP_INT_AUX_CH C P					
DP_INT_AUXCH		DP_85D	DISPLAYPORT	DP_INT_AUX_CH C N					
DP_INT_AUXCH		DP_85D	DISPLAYPORT	DP_INT_AUX_CH P					
DP_INT_AUXCH		DP_85D	DISPLAYPORT	DP_INT_AUX_CH N					
PCIE_85D		PCIE	PCIE	PCIE T29 R2D C P<3..0>					
PCIE_85D		PCIE	PCIE	PCIE T29 R2D C N<3..0>					
PCIE_PEG_D2R_LANE3		PCIE_85D	PCIE	PCIE T29 D2R P<3>					
PCIE_PEG_D2R_LANE2		PCIE_85D	PCIE	PCIE T29 D2R P<2>					
PCIE_PEG_D2R_LANE1		PCIE_85D	PCIE	PCIE T29 D2R P<1>					
PCIE_PEG_D2R_LANE0		PCIE_85D	PCIE	PCIE T29 D2R P<0>					
PCIE_PEG_D2R_LANE3		PCIE_85D	PCIE	PCIE T29 D2R N<3>					
PCIE_PEG_D2R_LANE2		PCIE_85D	PCIE	PCIE T29 D2R N<2>					
PCIE_PEG_D2R_LANE1		PCIE_85D	PCIE	PCIE T29 D2R N<1>					
PCIE_PEG_D2R_LANE0		PCIE_85D	PCIE	PCIE T29 D2R N<0>					
PCIE_PEG_R2D_LANE3		PCIE_85D	PCIE	PCIE T29 R2D P<3>					
PCIE_PEG_R2D_LANE2		PCIE_85D	PCIE	PCIE T29 R2D P<2>					
PCIE_PEG_R2D_LANE1		PCIE_85D	PCIE	PCIE T29 R2D P<1>					
PCIE_PEG_R2D_LANE0		PCIE_85D	PCIE	PCIE T29 R2D P<0>					
PCIE_PEG_R2D_LANE3		PCIE_85D	PCIE	PCIE T29 R2D N<3>					
PCIE_PEG_R2D_LANE2		PCIE_85D	PCIE	PCIE T29 R2D N<2>					
PCIE_PEG_R2D_LANE1		PCIE_85D	PCIE	PCIE T29 R2D N<1>					
PCIE_PEG_R2D_LANE0		PCIE_85D	PCIE	PCIE T29 R2D N<0>					
PCIE_85D		PCIE	PCIE	PCIE T29 D2R C P<3..0>					
PCIE_85D		PCIE	PCIE	PCIE T29 D2R C N<3..0>					
PCIE_CLK100M_T29		CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M T29 P					
PCIE_CLK100M_T29		CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M T29 N					
Clock Net Properties									
ELECTRICAL_CONSTRAINT_SET		NET_TYPE							
		PHYSICAL	SPACING						
SYSCLK_CLK32K_RTC		CLK_SLOW_55S	CLK_SLOW	SYSCLK_CLK32K_RTC					
SYSCLK_CLK25M_SB		CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_SB					
		CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_SB_R					
		CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_ENET					
		CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_ENET_R					
SYSCLK_CLK25M_T29		CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_T29					
		CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_T29_R					
PCH Constraints 2									
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## DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

## T29 I2C Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_12C_558	*	=55_OHM_SR	=55_OHM_SR	=55_OHM_SR	=55_OHM_SR	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_I2C	*	-2X_DIELECTRIC	?

## T29 SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_DP1_550	*	=55_OHM_SR	=55_OHM_SR	=55_OHM_SR	=55_OHM_SR	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_SFI	*	=2x_DIELECTRIC	?

## DP/T29 Connector Signal Constraints

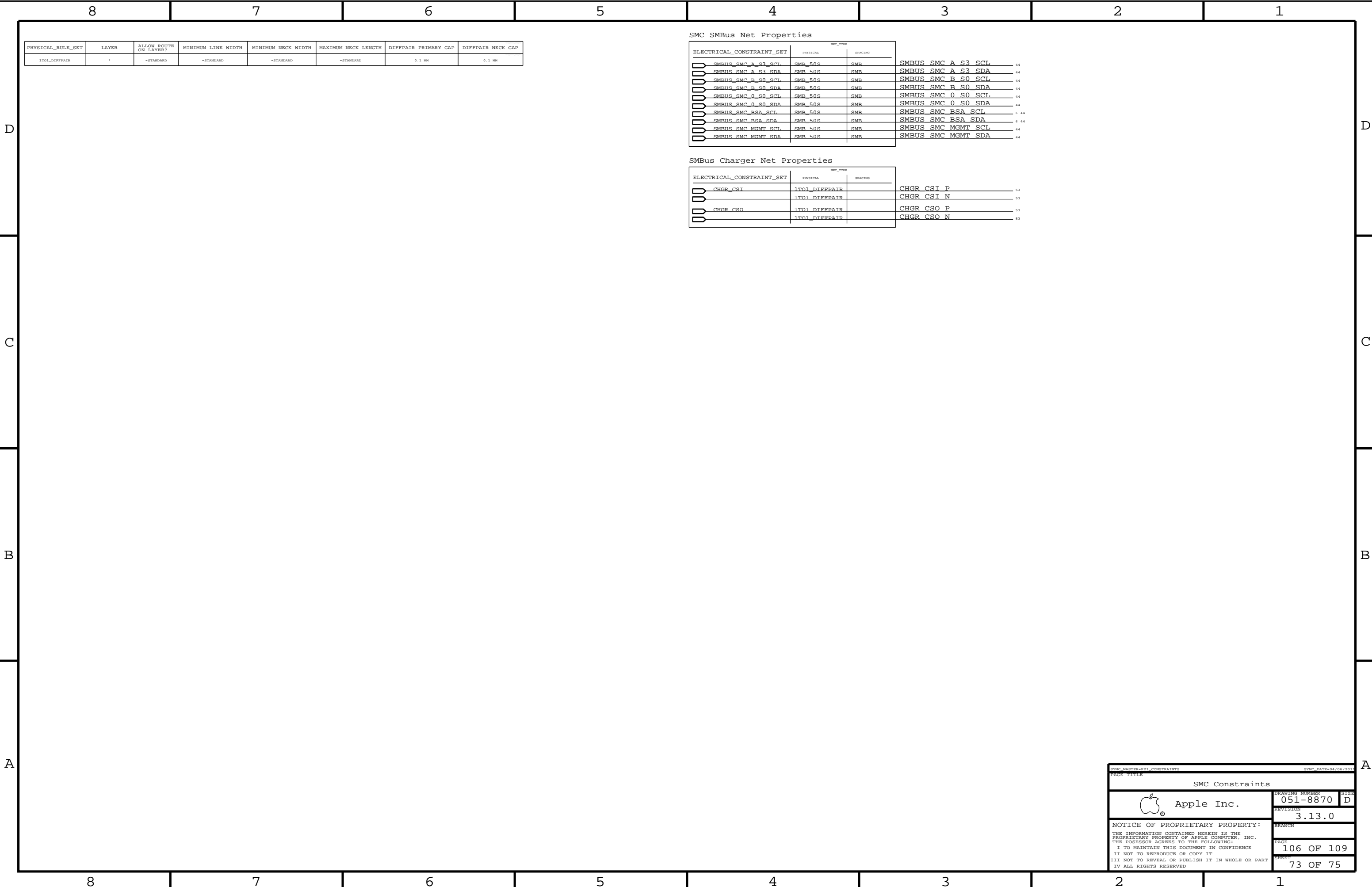
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29D_80D	*	+80_OHM_DIFF	-80_OHM_DIFF	+80_OHM_DIFF	+80_OHM_DIFF	+80_OHM_DIFF	+80_OHM_DIFF
T29D_100D	*	+100_OHM_DIFF	-100_OHM_DIFF	+100_OHM_DIFF	+100_OHM_DIFF	+100_OHM_DIFF	+100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29DP	*	=5x_DIELECTRIC	?	T29DP	TOP,BOTTOM	=7x_DIELECTRIC	?

SOURCE: Bill Cornelius's T29 Routing Notes

## T29 Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
DP		DP_85D	DISPLAYPORT	DP T29SNK0 ML C P<3..0>
DP		DP_85D	DISPLAYPORT	DP T29SNK0 ML C N<3..0>
DP	DP_T29SNK0_ML	DP_85D	DISPLAYPORT	DP T29SNK0 ML P<3..0>
DP	DP_T29SNK0_ML	DP_85D	DISPLAYPORT	DP T29SNK0 ML N<3..0>
DP		DP_85D	DISPLAYPORT	DP T29SNK0 AUXCH C P
DP		DP_85D	DISPLAYPORT	DP T29SNK0 AUXCH C N
DP	DP_T29SNK0_AUXCH	DP_85D	DISPLAYPORT	DP T29SNK0 AUXCH P
DP	DP_T29SNK0_AUXCH	DP_85D	DISPLAYPORT	DP T29SNK0 AUXCH N
DP		DP_85D	DISPLAYPORT	DP T29SNK1 ML C P<3..0>
DP		DP_85D	DISPLAYPORT	DP T29SNK1 ML C N<3..0>
DP	DP_T29SNK1_ML	DP_85D	DISPLAYPORT	DP T29SNK1 ML P<3..0>
DP	DP_T29SNK1_ML	DP_85D	DISPLAYPORT	DP T29SNK1 ML N<3..0>
DP		DP_85D	DISPLAYPORT	DP T29SNK1 AUXCH C P
DP		DP_85D	DISPLAYPORT	DP T29SNK1 AUXCH C N
DP	DP_T29SNK1_AUXCH	DP_85D	DISPLAYPORT	DP T29SNK1 AUXCH P
DP	DP_T29SNK1_AUXCH	DP_85D	DISPLAYPORT	DP T29SNK1 AUXCH N
DP				
DP		T29_I2C_55S	T29_I2C	I2C T29_SCL
DP		T29_I2C_55S	T29_I2C	I2C T29_SDA
DP	T29_SPI_CLK	T29_SPI_55S	T29_SPI	T29_SPI_CLK
DP	T29_SPI_MOSI	T29_SPI_55S	T29_SPI	T29_SPI_MOSI
DP	T29_SPI_MISO	T29_SPI_55S	T29_SPI	T29_SPI_MISO
DP	T29_SPI_CS_1	T29_SPI_55S	T29_SPI	T29_SPI_CS_L
DP				
DP		T29DP_80D	T29DP	T29_R2D C P<3..0>
DP		T29dp_80D	T29dp	T29_R2D C N<3..0>
DP		T29dp_80D	T29dp	T29_D2R P<3..0>
DP		T29dp_80D	T29dp	T29_D2R N<3..0>
DP				
DP	T29_R2D0	T29DP_80D	T29DP	T29_R2D P<0>
DP	T29_R2D0	T29dp_80D	T29dp	T29_R2D N<0>
DP	T29_R2D1	T29dp_80D	T29dp	T29_R2D P<1>
DP	T29_R2D1	T29DP_80D	T29DP	T29_R2D N<1>
DP		T29dp_80D	T29dp	T29_R2D C F P<1..0>
DP		T29dp_80D	T29dp	T29_R2D C F N<1..0>
DP	T29_D2R0	T29dp_80D	T29dp	T29_D2R C P<0>
DP	T29_D2R0	T29DP_80D	T29DP	T29_D2R C N<0>
DP	T29_D2R1	T29dp_80D	T29dp	T29_D2R C P<1>
DP	T29_D2R1	T29DP_80D	T29DP	T29_D2R C N<1>
DP		T29dp_80D	T29dp	T29DPA D2R1 AUXCH P
DP		T29dp_80D	T29dp	T29DPA D2R1 AUXCH N
DP				
DP		T29dp_80D	T29dp	DP SDRVA ML C P<3..0>
DP		T29dp_80D	T29dp	DP SDRVA ML C N<3..0>
DP		T29dp_80D	T29dp	DP SDRVA ML R P<3..0>
DP		T29dp_80D	T29dp	DP SDRVA ML R N<3..0>
DP	DP_SDRVA_ML_EVEN	T29dp_80D	T29dp	DP SDRVA ML P<0>
DP	DP_SDRVA_ML_EVEN	T29dp_80D	T29dp	DP SDRVA ML N<0>
DP	DP_SDRVA_ML_ODD	T29dp_80D	T29dp	DP SDRVA ML P<1>
DP	DP_SDRVA_ML_ODD	T29DP_80D	T29DP	DP SDRVA ML N<1>
DP	DP_SDRVA_ML_EVEN	T29dp_80D	T29dp	DP SDRVA ML P<2>
DP	DP_SDRVA_ML_EVEN	T29dp_80D	T29dp	DP SDRVA ML N<2>
DP	DP_SDRVA_ML_ODD	T29dp_80D	T29dp	DP SDRVA ML P<3>
DP	DP_SDRVA_ML_ODD	T29DP_80D	T29DP	DP SDRVA ML N<3>
DP	DP_SDRVA_AUXCH	T29dp_80D	T29dp	DP SDRVA AUXCH P
DP	DP_SDRVA_AUXCH	T29dp_80D	T29dp	DP SDRVA AUXCH N
DP		T29dp_80D	T29dp	DP SDRVA AUXCH C P
DP		T29dp_80D	T29dp	DP SDRVA AUXCH C N
DP				
DP	T29DPA_ML_ODD			T29DPA ML P<1>
DP	T29DPA_ML_ODD			T29DPA ML N<1>
DP	T29DPA_ML_ODD			T29DPA ML P<3>
DP	T29DPA_ML_ODD			T29DPA ML N<3>
DP		T29dp_80D	T29DP	T29DPA ML P<3..0>
DP		T29dp_80D	T29dp	T29DPA ML N<3..0>
DP		T29dp_80D	T29dp	T29DPA ML C P<3..0>
DP		T29dp_80D	T29dp	T29DPA ML C N<3..0>
DP	DP_A_EXT_AUXCH	T29dp_80D	T29dp	DP



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SMC Constraints

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1701_55S	*	+1:1_DIFFPAIR	+55_OHM_SR	+55_OHM_SR	+55_OHM_SR	+1:1_DIFFPAIR	+1:1_DIFFPAIR
THERM_1701_55S	*	+1:1_DIFFPAIR	+55_OHM_SR	+55_OHM_SR	+55_OHM_SR	+1:1_DIFFPAIR	+1:1_DIFFPAIR
DIFFPAIR	*	+1:1_DIFFPAIR			+1:1_DIFFPAIR	+1:1_DIFFPAIR	+1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	~2:1_SPACING	?
THERM	*	~2:1_SPACING	?
AUDIO	*	~2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENRT_MDI	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	= STANDARD	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPER1	NET_SPACING_TYPER2	AREA_TYPER	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2046
PCIE	GND	*	GND_P2046
SATA	GND	*	GND_P2046
USB	GND	*	GND_P2046
CLK_PCIE	SR_POWER	*	PWR_P2046
SATA	SR_POWER	*	PWR_P2046
USB	SR_POWER	*	PWR_P2046

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLE	QND	*	QND_P2PM
MEM_CMD	QND	*	QND_P2PM
MEM_CTRL	QND	*	QND_P2PM
MEM_DATA	QND	*	QND_P2PM
MEM_DQS	QND	*	QND_P2PM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MDX_400 OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
MDX_720 OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
MDX_370 OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
MDX_850 OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_850 OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.076 MM OVERRIDE	10 MM OVERRIDE	OVERRIDE	OVERRIDE
USB_850 OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	800 MIL OVERRIDE	OVERRIDE	OVERRIDE
CPU_2704S OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
CLK_PCIE_900 OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE

ELECTRICAL_CONSTRAINT_SET		PROTOCOL	INTERFACE	
		ENET_100D	ENETCONN	ENETCONN P<3..0>
		ENET_100D	ENETCONN	ENETCONN N<3..0>
		SATA_90D	SATA	SATA ODD D2R UF P
		SATA_90D	SATA	SATA ODD D2R UF N
		SATA_90D	SATA	SATA HDD D2R RDRV R OUT P
		SATA_90D	SATA	SATA HDD D2R RDRV R OUT N
		SATA_90D	SATA	SATA HDD R2D RDRV R IN P
		SATA_90D	SATA	SATA HDD R2D RDRV R IN N
		SATA_90D	SATA	SATA HDD D2R RDRV R IN P
		SATA_90D	SATA	SATA HDD D2R RDRV R IN N
		SATA_90D	SATA	SATA HDD R2D RDRV R OUT P
		SATA_90D	SATA	SATA HDD R2D RDRV R OUT N
	SENSE_DIFFPAIR	THERM_170I_55S	THERM	CPUTHMSNS D2 P
		THERM_170I_55S	THERM	CPUTHMSNS D2 N
	CPU_THERMD	THERM_170I_55S	THERM	CPU THERMD P
		THERM_170I_55S	THERM	CPU THERMD N
	SENSE_DIFFPAIR	THERM_170I_55S	THERM	T29 THERMD P
		THERM_170I_55S	THERM	T29 THERMD N
	SENSE_DIFFPAIR	THERM_170I_55S	THERM	T29 MLBBOT THMSNS P
		THERM_170I_55S	THERM	T29 MLBBOT THMSNS N
	SENSE_DIFFPAIR	SENSE_170I_55S	SENSE	ISNS HS COMPUTING N
		SENSE_170I_55S	SENSE	ISNS HS COMPUTING P
	SENSE_DIFFPAIR	SENSE_170I_55S	SENSE	ISNS HS OTHER N
		SENSE_170I_55S	SENSE	ISNS HS OTHER P
	SENSE_DIFFPAIR	SENSE_170I_55S	SENSE	CPUVCCIOS0 CS N
		SENSE_170I_55S	SENSE	CPUVCCIOS0 CS P
	SENSE_DIFFPAIR	SENSE_170I_55S	SENSE	CPUIMVP ISNS1 P
		SENSE_170I_55S	SENSE	CPUIMVP ISNS1 N
	SENSE_DIFFPAIR	SENSE_170I_55S	SENSE	CPUIMVP ISNS2 P
		SENSE_170I_55S	SENSE	CPUIMVP ISNS2 N
	SENSE_DIFFPAIR	SENSE_170I_55S	SENSE	CPUIMVP ISNS1G P
		SENSE_170I_55S	SENSE	CPUIMVP ISNS1G N
	SENSE_DIFFPAIR	SENSE_170I_55S	SENSE	CPUIMVP ISUM R P
		SENSE_170I_55S	SENSE	CPUIMVP ISUM R N
	SENSE_DIFFPAIR	SENSE_170I_55S	SENSE	CPUIMVP ISUMG R P
		SENSE_170I_55S	SENSE	CPUIMVP ISUMG R N
	SENSE_DIFFPAIR	SENSE_170I_55S	SENSE	CPUIMVP ISNS P
		SENSE_170I_55S	SENSE	CPUIMVP ISNS N
	SENSE_DIFFPAIR	SENSE_170I_55S	SENSE	VCCSA0 CS P
		SENSE_170I_55S	SENSE	VCCSA0 CS N
	SENSE_DIFFPAIR	SENSE_170I_55S	SENSE	CPUIMVP ISUMG P
		SENSE_170I_55S	SENSE	CPUIMVP ISUMG N
	SENSE_DIFFPAIR	SENSE_170I_55S	SENSE	ISNS CPU N
		SENSE_170I_55S	SENSE	ISNS CPU P
	SENSE_DIFFPAIR	SENSE_170I_55S	SENSE	ISNS HDD N
		SENSE_170I_55S	SENSE	ISNS HDD P
	SENSE_DIFFPAIR	SENSE_170I_55S	SENSE	ISNS HDD R N
		SENSE_170I_55S	SENSE	ISNS HDD R P
	SENSE_DIFFPAIR	SENSE_170I_55S	SENSE	ISNS LCDBKLT N
		SENSE_170I_55S	SENSE	ISNS LCDBKLT P
	SENSE_DIFFPAIR	SENSE_170I_55S	SENSE	ISNS ODD N
		SENSE_170I_55S	SENSE	ISNS ODD P
	SENSE_DIFFPAIR	SENSE_170I_55S	SENSE	ISNS ODD R N
		SENSE_170I_55S	SENSE	ISNS ODD R P
	SENSE_DIFFPAIR	SENSE_170I_55S	SENSE	ISNS I1V5 S3 N
		SENSE_170I_55S	SENSE	ISNS I1V5 S3 P
	SENSE_DIFFPAIR	SENSE_170I_55S	SENSE	ISNS P1V8GPU R N
		SENSE_170I_55S	SENSE	ISNS P1V8GPU R P
	SENSE_DIFFPAIR	SENSE_170I_55S	SENSE	ISNS AIRPORT N
		SENSE_170I_55S	SENSE	ISNS AIRPORT P
	I1VDS_90D	I1VDS		LVDS CONN A CLK F N
	I1VDS_90D	I1VDS		LVDS CONN A CLK F P

## Audio Net Properties

		NET_TYPE		
ELECTRICAL_CONSTRAINT_SET		PHYSICAL	SPACING	
<b>NAME</b>	SPKRAMP_INR	DIEFFPAIR	AUDIO	SPKRAMP_INR_P 6 40 51 74
<b>NAME</b>		DIEFFPAIR	AUDIO	SPKRAMP_INR_N 6 40 51 74
<b>NAME</b>	MAX98300_R	DIEFFPAIR	AUDIO	MAX98300_R_P 51
<b>NAME</b>		DIEFFPAIR	AUDIO	MAX98300_R_N 51


K21/K78 Specific Net Properties		NET_TYPES	
ELECTRICAL_CONSTRAINT_SET	PROPERTIES	PROPERTIES	
PCIE CLK100M AP	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M AP CONN_P
	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M AP CONN_N
	1T01_DIFFEPAIR		CHGR CSI R P
	1T01_DIFFEPAIR		CHGR CSI R N
	1T01_DIFFEPAIR		CHGR CSO R P
	1T01_DIFFEPAIR		CHGR CSO R N
(USB_EFSTA)	USB_85D	USB	USB2 EXTA MUXED P
(USB_EFSTA)	USB_85D	USB	USB2 EXTA MUXED N
(USB_EFSTA)	USB_85D	USB	USB2 LT1 P
(USB_EFSTA)	USB_85D	USB	USB2 LT1 N
	USB_85D	USB	CONN USB2 BT P
	USB_85D	USB	CONN USB2 BT N
	USB_85D	USB	USB LT2 P
	USB_85D	USB	USB LT2 N
	DP_85D	DISPLAYPORT	DP IG AUX CH C P
	DP_85D	DISPLAYPORT	DP IG AUX CH C N
SPK_OUT	DIFFEPAIR	AUDIO	SPKRAMP L P_OUT
SPK_OUT	DIFFEPAIR	AUDIO	SPKRAMP L N_OUT
SPK_OUT	DIFFEPAIR	AUDIO	SPKRAMP SUB P_OUT
SPK_OUT	DIFFEPAIR	AUDIO	SPKRAMP SUB N_OUT
SPK_OUT	DIFFEPAIR	AUDIO	SPKRAMP R P_OUT
SPK_OUT	DIFFEPAIR	AUDIO	SPKRAMP R N_OUT
AUD_DIFF	1T01_DIFFEPAIR	AUDIO	SSM2315 SUB_N
AUD_DIFF	1T01_DIFFEPAIR	AUDIO	SSM2315 SUB_P
AUD_DIFF	1T01_DIFFEPAIR	AUDIO	SSM2315 L_N
AUD_DIFF	1T01_DIFFEPAIR	AUDIO	SSM2315 L_P
AUD_DIFF	1T01_DIFFEPAIR	AUDIO	SSM2315 R_N
AUD_DIFF	1T01_DIFFEPAIR	AUDIO	SSM2315 R_P
AUD_DIFF	1T01_DIFFEPAIR	AUDIO	AUD LO2 N_R
AUD_DIFF	1T01_DIFFEPAIR	AUDIO	AUD LO2 P_R
AUD_DIFF	1T01_DIFFEPAIR	AUDIO	AUD LO1 N_R
AUD_DIFF	1T01_DIFFEPAIR	AUDIO	AUD LO1 P_R
AUD_DIFF	1T01_DIFFEPAIR	AUDIO	AUD LO2 N_L
AUD_DIFF	1T01_DIFFEPAIR	AUDIO	AUD LO2 P_L
AUD_DIFF	1T01_DIFFEPAIR	AUDIO	SPKRAMP INL_P
AUD_DIFF	1T01_DIFFEPAIR	AUDIO	SPKRAMP INL_N
SPKRAMP_INR	DIFFEPAIR	AUDIO	SPKRAMP_INR_P
AUD_DIFF	DIFFEPAIR	AUDIO	SPKRAMP_INR_N
AUD_DIFF	1T01_DIFFEPAIR	AUDIO	SPKRAMP_INSUB_P
AUD_DIFF	1T01_DIFFEPAIR	AUDIO	SPKRAMP_INSUB_N
	USB_85D	USB	USB_TPAD_R_P
	USB_85D	USB	USB_TPAD_R_N
		SR_POWER	PP3V3_S5
		SR_POWER	PP3V3_S0
		GND	GND


Misc Net Properties	
ELECTRICAL_CONSTRAINT_SET	NET_TYPE
	PHYSICAL      SPACING
<b>USB_MUX</b> (USB_EXTA)	USB_R5D      USBR      USB EXTA MUXED P
<b>USB_MUX</b> (USB_EXTA)	USB_R5D      USBR      USB EXTA MUXED N
<b>USB_MUX</b> (USB_EXTA)	USB_R5D      USBR      USB LT1 P
<b>USB_MUX</b> (USB_EXTA)	USB_R5D      USBR      USB LT1 N
<b>USB_TPAD</b> (USB_TPAD)	USB_R5D      USBR      USB TPAD CONN P
<b>USB_TPAD</b> (USB_TPAD)	USB_R5D      USBR      USB TPAD CONN N
<b>SMBUS_SMC_MGMT_SDA</b>	SMB_55S      SMBR      I2C SMC SMS SDA R
<b>SMBUS_SMC_MGMT_SCL</b>	SMB_55S      SMBR      I2C SMC SMS SCL R
<b>TCON_SCL</b>	SMB_55S      SMBR      I2C TCON_SCL
<b>TCON_SDA</b>	SMB_55S      SMBR      I2C TCON_SDA
<b>TCON_SCL_CONN</b>	SMB_55S      SMBR      I2C TCON_SCL_CONN
<b>TCON_SDA_CONN</b>	SMB_55S      SMBR      I2C TCON_SDA_CONN

## Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for ARD fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_72D	BOTTOM			0.127 MM	6.35 MM		
MEM_85D	TOP			0.1 MM	6.35 MM		

BMC MASTER-#21 CONSTRAINTS		BMC DATE=04/08/2011	
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Project Specific Constraints			
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K90i Board-Specific Spacing & Physical Constraints							
BOARD LAYERS			BOARD AREAS			BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM			NO_TYPE, BGA			MM	15.5.1
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP, BOTTOM	Y	0.110 MM	0.090 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP, BOTTOM	Y	0.170 MM	0.170 MM			
40_OHM_SE	ISL3, ISL4, ISL9, ISL10	Y	0.140 MM	0.140 MM	=STANDARD	=STANDARD	=STANDARD
40_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP, BOTTOM	Y	0.195 MM	0.1 MM			
37_OHM_SE	ISL3, ISL4, ISL9, ISL10	Y	0.160 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD
37_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP, BOTTOM	Y	0.310 MM	0.2 MM			
27P4_OHM_SE	*	Y	0.250 MM	0.2 MM	=STANDARD	=STANDARD	=STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP, BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3, ISL10	Y	0.135 MM	0.135 MM		0.130 MM	0.130 MM
72_OHM_DIFF	ISL4, ISL9	Y	0.155MM	0.155 MM		0.130 MM	0.130 MM
72_OHM_DIFF	TOP, BOTTOM	Y	0.165 MM	0.165 MM		0.130 MM	0.130 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3, ISL10	Y	0.095 MM	0.1 MM		0.170 MM	0.170 MM
85_OHM_DIFF	ISL4, ISL9	Y	0.115 MM	0.115 MM		0.170 MM	0.170 MM
85_OHM_DIFF	TOP, BOTTOM	Y	0.130 MM	0.130 MM		0.195 MM	0.195 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3, ISL10	Y	0.089 MM	0.089 MM		0.210 MM	0.210 MM
90_OHM_DIFF	ISL4, ISL9	Y	0.105 MM	0.105 MM		0.210 MM	0.210 MM
90_OHM_DIFF	TOP, BOTTOM	Y	0.115 MM	0.115 MM		0.210 MM	0.210 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3, ISL10	Y	0.074 MM	0.074 MM		0.250 MM	0.250 MM
100_OHM_DIFF	ISL4, ISL9	Y	0.085 MM	0.085 MM		0.250 MM	0.250 MM
100_OHM_DIFF	TOP, BOTTOM	Y	0.091 MM	0.091 MM		0.200 MM	0.200 MM
NOTE: 110_DIFF is 110-ohms differential impedance on outer layers and 105-ohms on inner layers.							
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3, ISL10	N	0.070 MM	0.070 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL4, ISL9	Y	0.071 MM	0.071 MM		0.300 MM	0.300 MM
110_OHM_DIFF	TOP, BOTTOM	Y	0.077 MM	0.077 MM		0.280 MM	0.280 MM
NOTE: These are Intel recommended impedances for PEG, unused on K90i.							
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
48_OHM_SE	TOP, BOTTOM	Y	0.120 MM	0.165 MM			
48_OHM_SE	*	Y	0.097 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3, ISL10	Y	0.110 MM	0.110 MM		0.170 MM	0.170 MM
80_OHM_DIFF	ISL4, ISL9	Y	0.129 MM	0.129 MM		0.170 MM	0.170 MM
80_OHM_DIFF	TOP, BOTTOM	Y	0.145 MM	0.145 MM		0.180 MM	0.180 MM
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DEFAULT	*	0.1 MM	?	*	*	BGA	BGA_P1MM
STANDARD	*	=DEFAULT	?	MEM_CLK	*	BGA	BGA_P2MM
BGA_P1MM	*	=DEFAULT	?	CLK_PCIE	*	BGA	BGA_P2MM
BGA_P2MM	*	=DEFAULT	?	CLK_SLOW	*	BGA	BGA_P2MM
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?	2X_DIELECTRIC	*	0.140 MM	?
2:1_SPACING	*	0.2 MM	?	3X_DIELECTRIC	*	0.210 MM	?
2.5:1_SPACING	*	0.25 MM	?	4X_DIELECTRIC	*	0.280 MM	?
3:1_SPACING	*	0.3 MM	?	5X_DIELECTRIC	*	0.350 MM	?
4:1_SPACING	*	0.4 MM	?	7X_DIELECTRIC	*	0.490 MM	?
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_DIFF_BGA	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
85_DIFF_BGA	ISL3, ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
85_DIFF_BGA	ISL9, ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
NOTE: 85_DIFF_BGA is 85-ohms differential impedance on outer layers and 80-ohms on inner layers.							
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_DIFF_BGA	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
90_DIFF_BGA	ISL3, ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
90_DIFF_BGA	ISL9, ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
NOTE: 90_DIFF_BGA is 90-ohms differential impedance on outer layers and 85-ohms on inner layers.							
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3, ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9, ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.							
SYNOPSIS: MATERIALS CONSTRAINTS							
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